- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

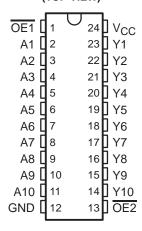
description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

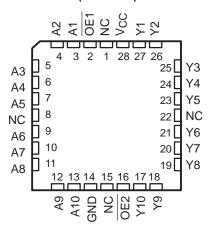
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable $(\overline{OE1} \text{ or } \overline{OE2})$ input is high, all ten outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

The SN54BCT29827B is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT29827B is characterized for operation from 0°C to 70°C.

SN54BCT29827B ... JT OR W PACKAGE SN74BCT29827B ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT29827B . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

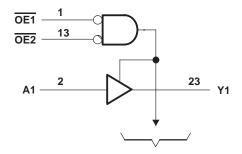
FUNCTION TABLE

	INPUTS	OUTPUT			
OE1	OE2	Α	Y		
L	L	L	L		
L	L	Н	Н		
Н	X	Χ	Z		
Χ	Н	Χ	Z		

logic symbol†

OE1 ΕN 13 OE2 23 Α1 **Y1** 22 A2 **Y2** 4 21 **Y3 A3** 5 20 Α4 **Y4** 6 19 **A5 Y5** 7 18 **Y6** A6 8 17 **A7 Y7** 16 **Y8 A8** 10 15 A9 Υ9 11 14 Y10 A10

logic diagram (positive logic)



To Nine Other Channels

Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V _O	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, V _O	-0.5 V to V_{CC}
Input clamp current, $I_{ K }(V_{ } < 0)$	30 mA
Current into any output in the low state, IO: SN54BCT29827B	48 mA
SN74BCT29827B	96 mA
Operating free-air temperature range: SN54BCT29827B –	55°C to 125°C
SN74BCT29827B	0°C to 70 °C
Storage temperature range –	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54BCT29827B		SN74BCT29827B			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
lik	Input clamp current			-18			-18	mA
loh	High-level output current			-15			-24	mA
loL	Low-level output current			24			48	mA
TA	Operating free-air temperature	-55		125	0		70	°C



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			4BCT298	27B	SN74BCT29827B			UNIT	
PARAMETER	15:	51 CONDITIONS	MIN	TYP†	MAX	MIN	TYP [†]	MAX	ONIT	
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V	
	V _{CC} = 4.5 V	$I_{OH} = -15 \text{ mA}$	2	3.2		2.4	3.3			
Voн	vCC = 4.5 v	$I_{OH} = -24 \text{ mA}$				2	3.1		V	
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -3 \text{ mA}$				2.7				
Voi	V00 - 4 5 V	I _{OL} = 24 mA		0.38	0.55				V	
VOL	V _{CC} = 4.5 V	$I_{OL} = 48 \text{ mA}$					0.42	0.5	٧	
lį	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA	
lін	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ	
I _{IL}	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V			-0.2			-0.2	mA	
los [‡]	$V_{CC} = 5.5 \text{ V},$	$V_O = 0$	-75		-250	-75		-250	mA	
lozh	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.7 \text{ V}$			20			20	μΑ	
lozL	$V_{CC} = 5.5 \text{ V},$	V _O = 0.5 V			-20			-20	μΑ	
ICCL	$V_{CC} = 5.5 \text{ V},$	Outputs open		28			28	40	mA	
Іссн	$V_{CC} = 5.5 \text{ V},$	Outputs open		15			15	25	mA	
Iccz	$V_{CC} = 5.5 \text{ V},$	Outputs open		3.5			3.5	6	mA	
Ci	$V_{CC} = 5 V$,	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$		6			6		pF	
Co	V _{CC} = 5 V,	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		8			8		pF	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54BCT29827B		SN74BCT29827B		UNIT
	(INPOT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	А	Y	1.6	3.3	5.3	1.6	5.5	1.6	5.5	ns
^t PHL			2.7	5.1	7.3	2.7	7.7	2.7	7.5	115
^t PZH		OE Y	2.7	5.3	7.9	2.7	10.6	2.7	9.1	
t _{PZL}	OE		5.3	8.5	12.1	5.3	13.5	5.3	12.8	ns
^t PHZ	ŌĒ	OE V	2.8	5.4	8.2	2.8	9.4	2.8	8.8	
t _{PLZ}		Y	2.3	5.1	7.6	2.3	9.1	2.3	8.4	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74BCT29827BDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT29827BDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT29827BDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT29827BNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT29827BNTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

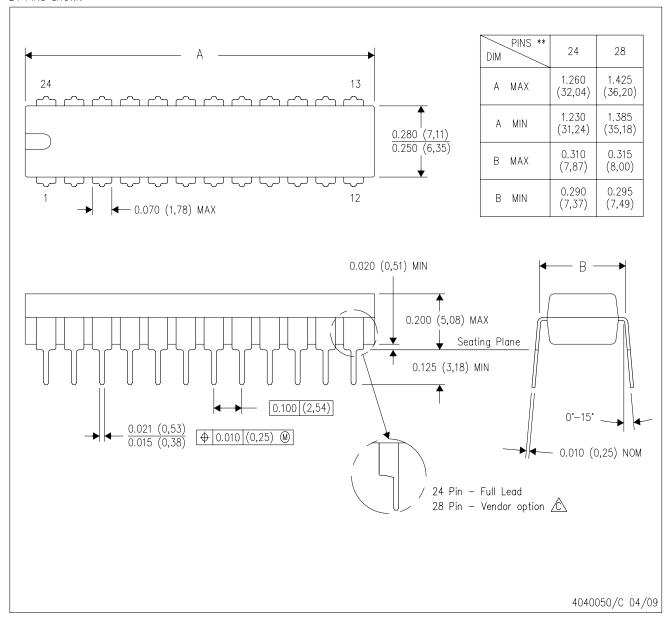
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NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

The 28 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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