



# STD12NF06-1 STD12NF06

N-channel 60V - 0.08Ω - 12A - DPAK - IPAK  
STripFET™ II Power MOSFET

## General features

Type	V <sub>DSSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD12NF06	60V	<0.1Ω	12A
STD12NF06-1	60V	<0.1Ω	12A

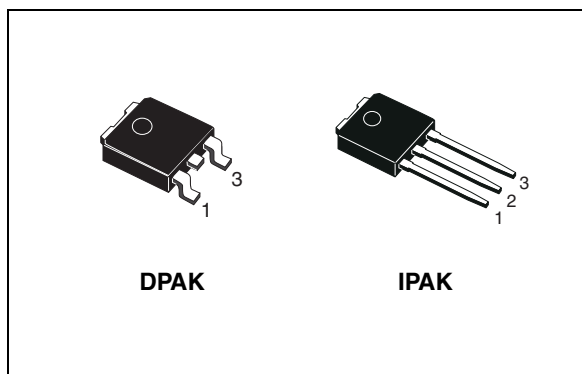
- Exceptional dv/dt capability
- Low gate charge

## Description

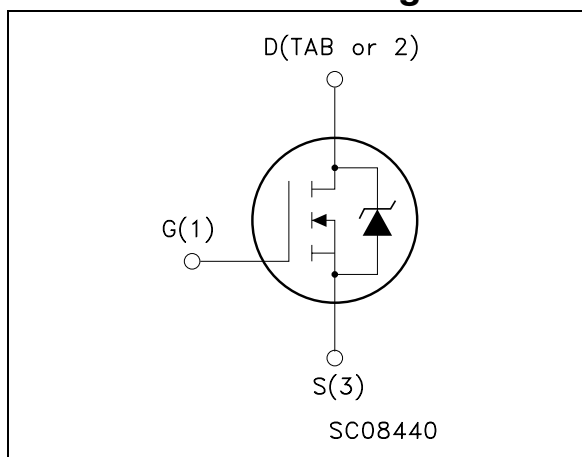
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD12NF06T4	D12NF06	DPAK	Tape & reel
STD12NF06-1	D12NF06	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	12	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	8.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	30	W
	Derating factor	0.2	W/ $^\circ C$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	140	mJ
$T_{stg}$	Storage temperature	-55 to 175	$^\circ C$
$T_J$	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 12A$ ,  $di/dt \leq 200A/\mu s$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$
3. Starting  $T_J = 25^\circ C$ ,  $I_D = 6A$ ,  $V_{DD} = 30V$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	5	$^\circ C/W$
$R_{thJA}$	Thermal resistance junction-ambient Max	100	$^\circ C/W$
$T_I$	Maximum lead temperature for soldering purpose	275	$^\circ C$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25mA, V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 6A$		0.08	0.1	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 6A$		5		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		315		pF
$C_{oss}$	Output capacitance			70		pF
$C_{rss}$	Reverse transfer capacitance			30		pF
$Q_g$	Total gate charge	$V_{DD} = 48V, I_D = 12A$ $V_{GS} = 10V$		10	12	nC
$Q_{gs}$	Gate-source charge			3.0		nC
$Q_{gd}$	Gate-drain charge			3.5		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30V, I_D = 6A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		7		ns
$t_r$	Rise time			18		ns
$t_{d(off)}$	Turn-off delay time			17		ns
$t_f$	Fall time			6		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				12	A
$I_{SDM}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 30V, T_J = 150^\circ C$ <a href="#">Figure 15 on page 8</a>		50		ns
$Q_{rr}$	Reverse recovery charge			65		$\mu C$
$I_{RRM}$	Reverse recovery current			3.5		A

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

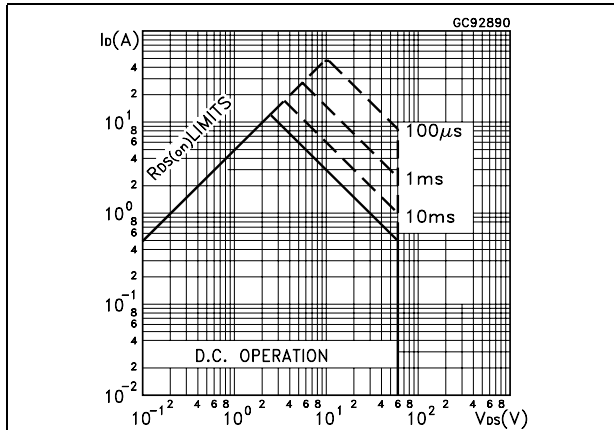


Figure 2. Thermal impedance

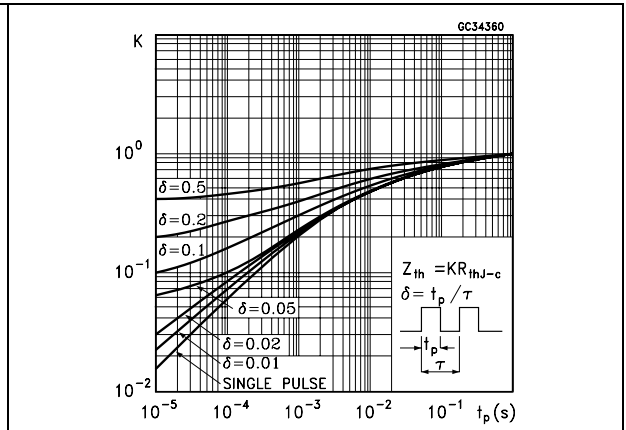


Figure 3. Output characteristics

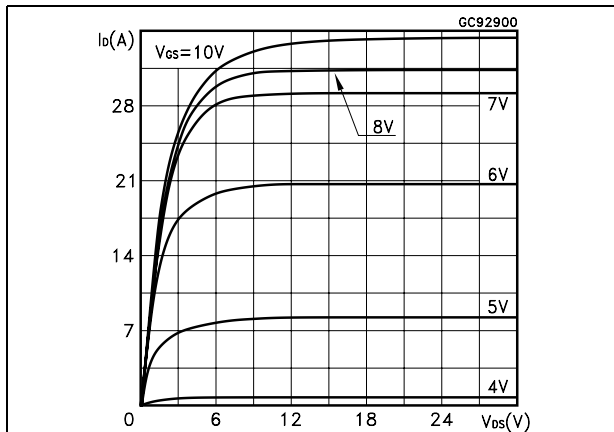


Figure 4. Transfer characteristics

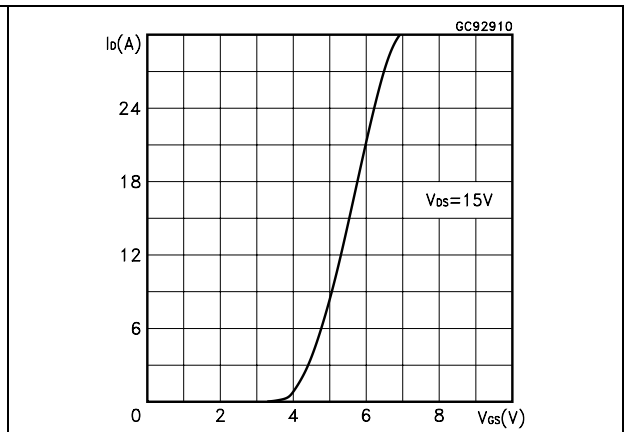


Figure 5. Transconductance

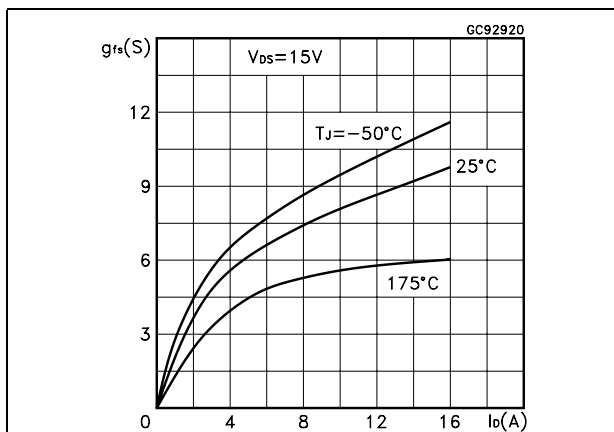


Figure 6. Static drain-source on resistance

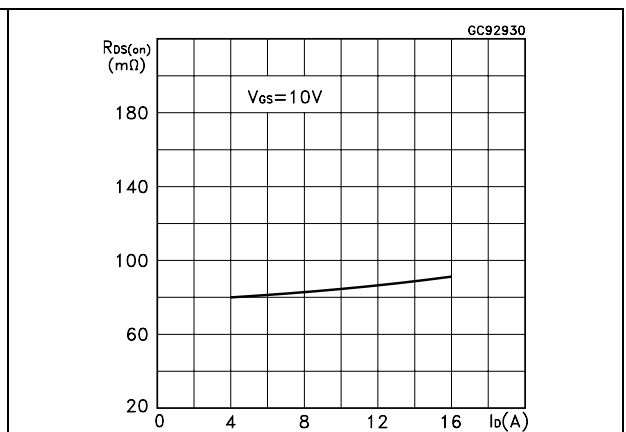


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

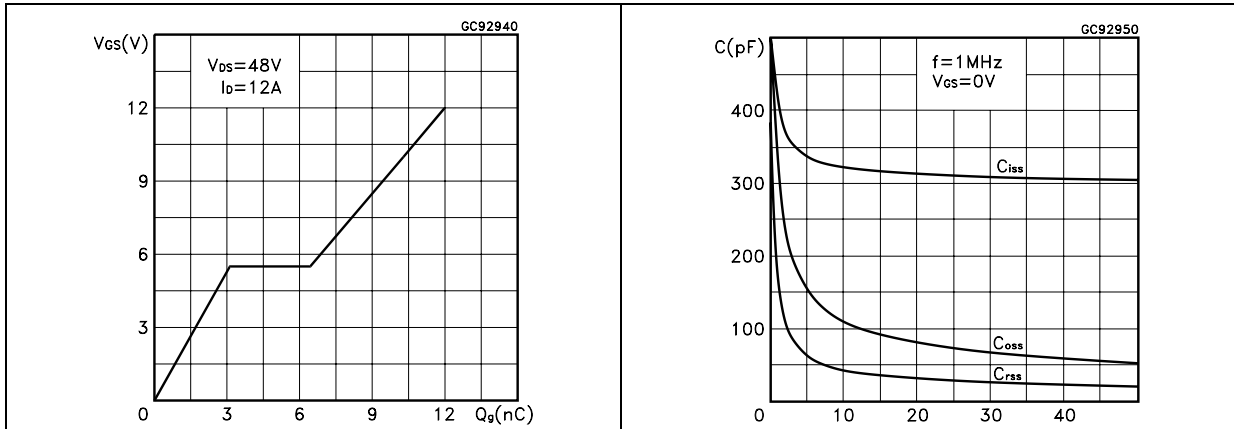


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

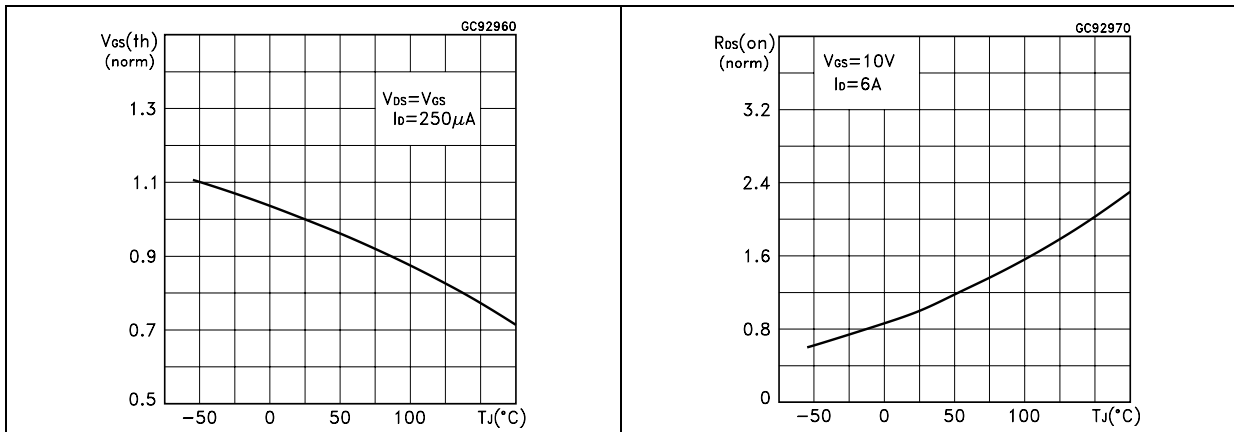
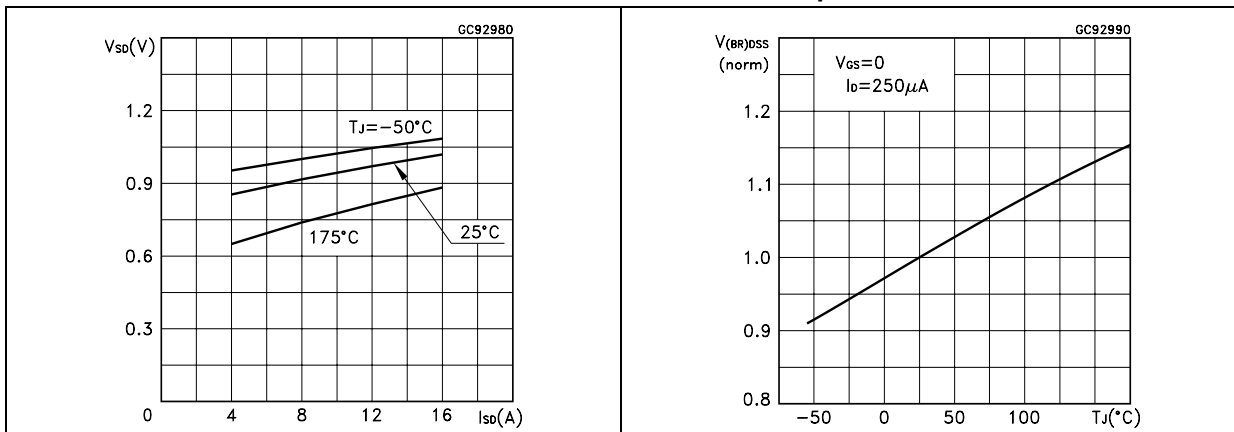


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs. temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

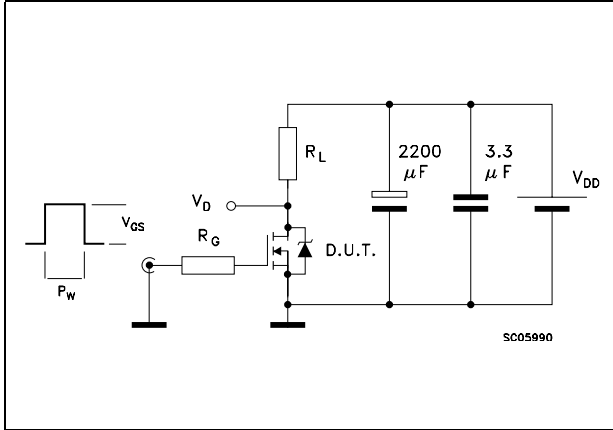


Figure 14. Gate charge test circuit

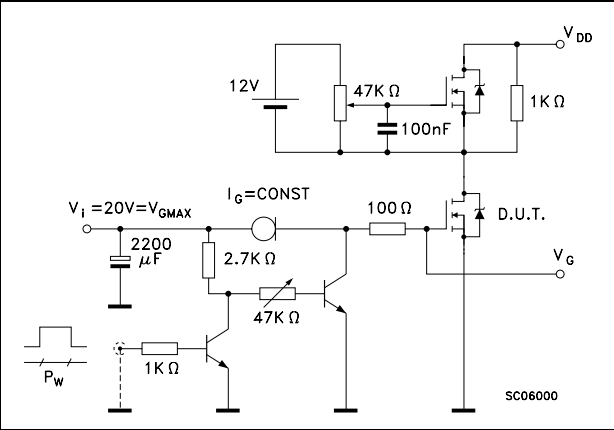


Figure 15. Test circuit for inductive load switching and diode recovery times

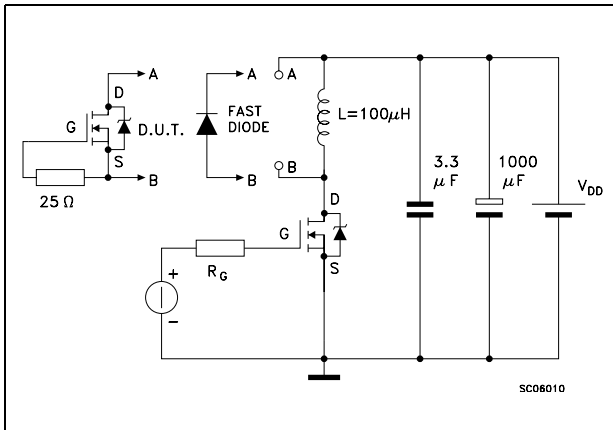


Figure 16. Unclamped Inductive load test circuit

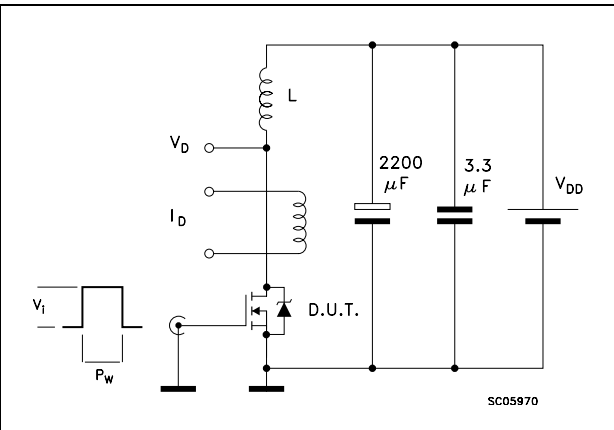
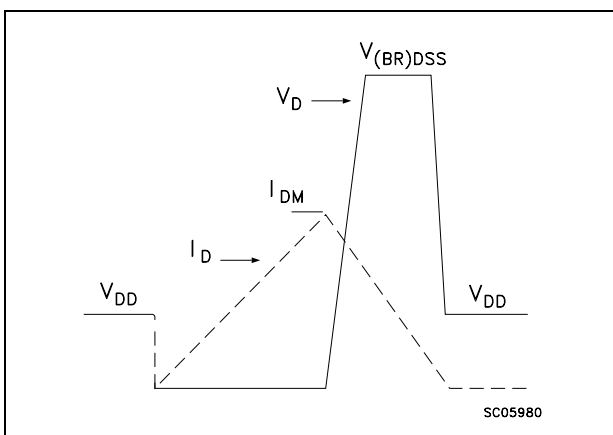


Figure 17. Unclamped inductive waveform



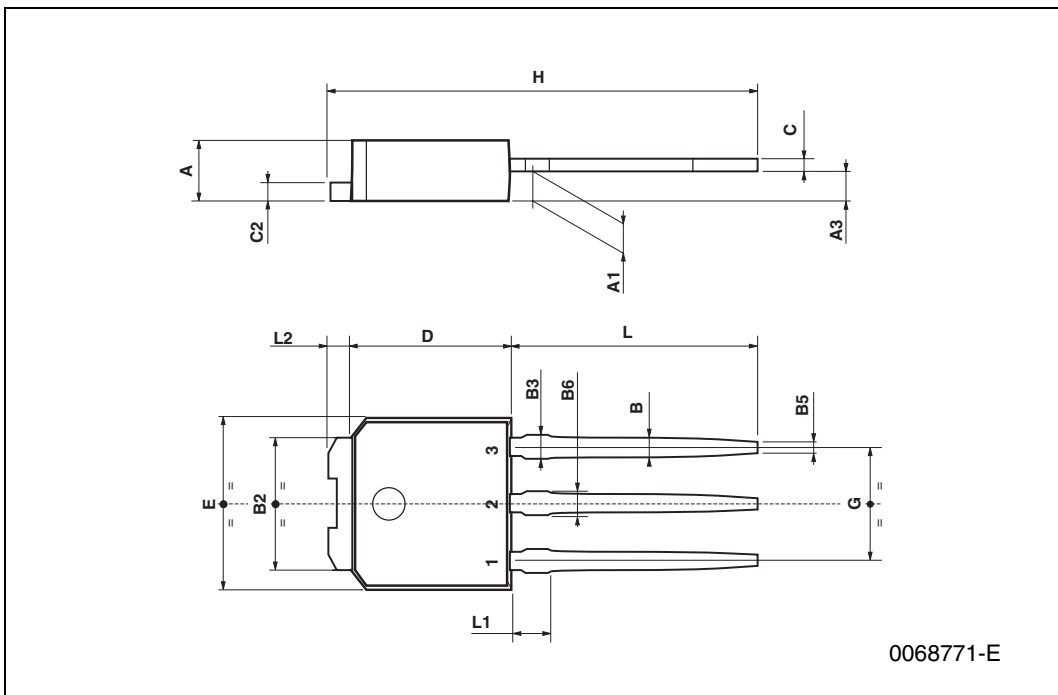


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

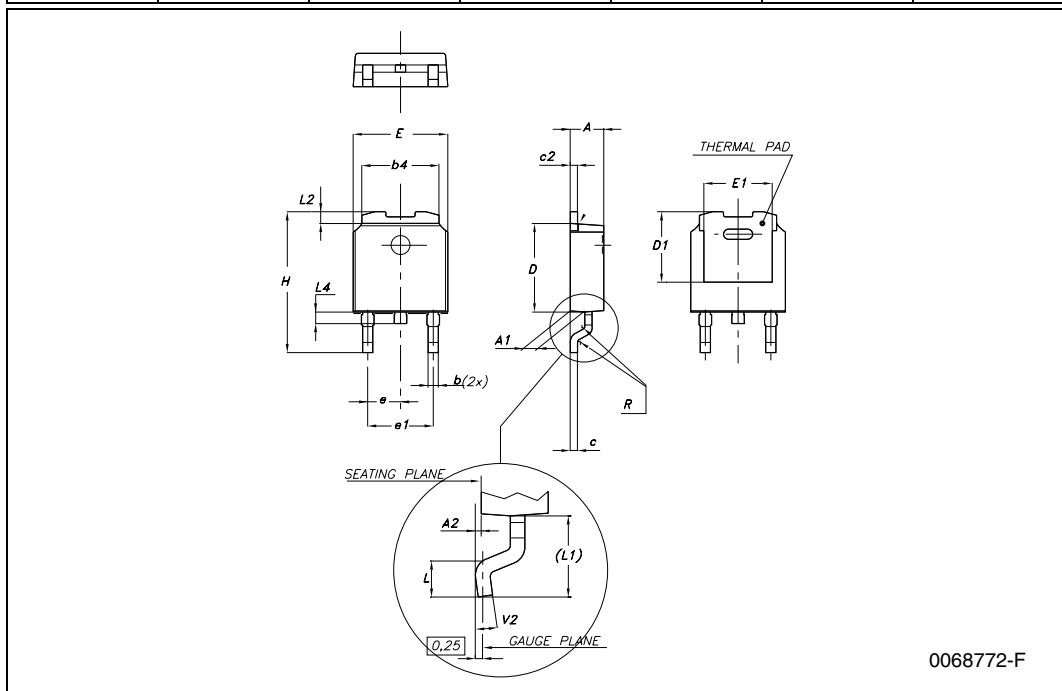
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



**DPAK MECHANICAL DATA**

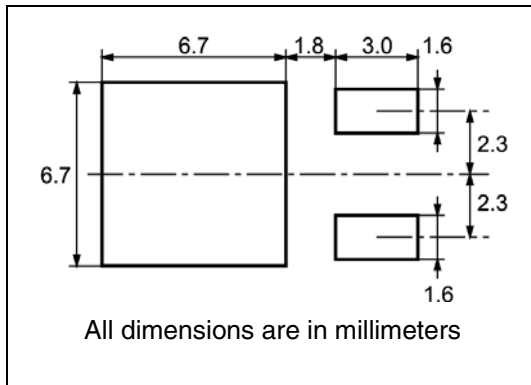
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

## 6 Revision history

**Table 7. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
09-Sep-2004	3	Complete document
07-Aug-2006	4	The document has been reformatted
19-Feb-2007	5	Typo mistake on page 1

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