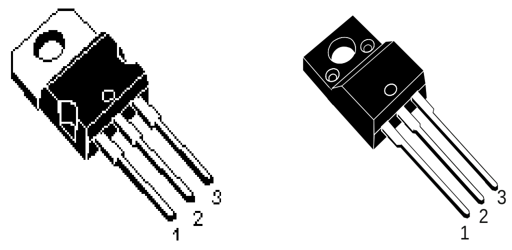
N-CHANNEL 300V - 0.80Ω - 5A TO-220/TO-220FP Zener-Protected SuperMESH™MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STP7NK30Z STF7NK30Z	300 V 300 V	< 0.9 Ω < 0.9 Ω	5 A 5 A	50 W 20 W

- TYPICAL R_{DS}(on) = 0.80 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

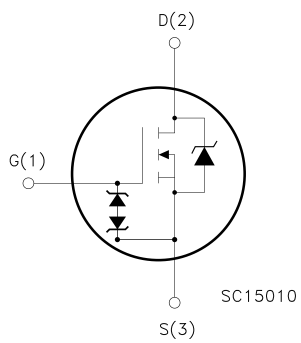
Figure 1: Package



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ product

Figure 2: Internal Schematic Diagram



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STF7NK30Z	F7NK30Z	TO-220FP	TUBE
STP7NK30Z	P7NK30Z	TO-220	TUBE

Rev. 2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		STP7NK30Z	STF7NK30Z	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	300		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	300		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at T_C = 25°C	5	5 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	3.2	3.2 (*)	A
I_{DM} (•)	Drain Current (pulsed)	20	20 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	50	20	W
	Derating Factor	0.4	0.16	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2800		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(●) Pulse width limited by safe operating area
(1) I_{SD} ≤5.7A, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	2.50	6.25	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	130	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D =1 mA, V_{GS} = 0	300			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 2.5 A		0.80	0.90	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =15 V, I_D = 2.5 A		2.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		380 74 15		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		30		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	V_{DD} = 425 V, I_D = 2.8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 18)		11 25 20 10		ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 320V, I_D = 5A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 17)		8.5 8.5 20		ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 320V, I_D = 5 A, V_{GS} = 10V (see Figure 21)		13 4.5 7.6	17	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				5 20	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 5 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5 A, di/dt = 100A/µs V_{DD} = 40, T_j = 150°C (see Figure 19)		154 716 9.3		ns nC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Figure 3: Safe Operating Area for TO-220

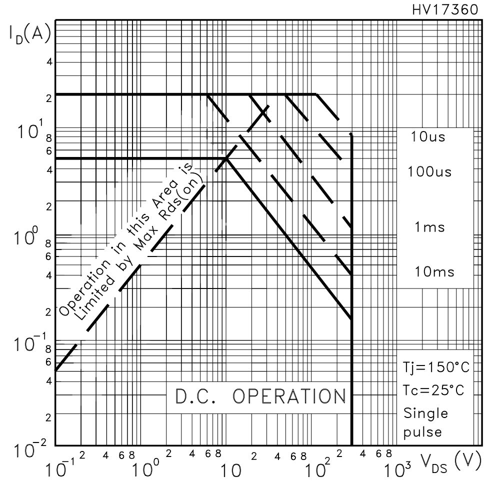


Figure 6: Thermal Impedance for TO-220

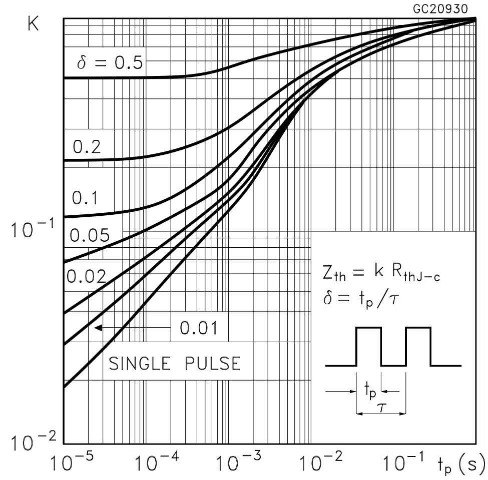


Figure 4: Safe Operating Area for TO-220FP

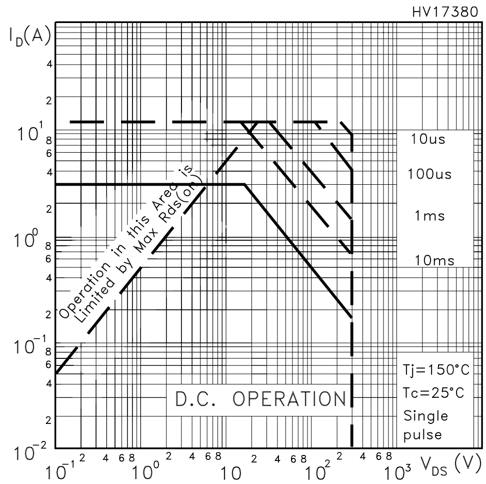


Figure 7: Thermal Impedance for TO-220FP

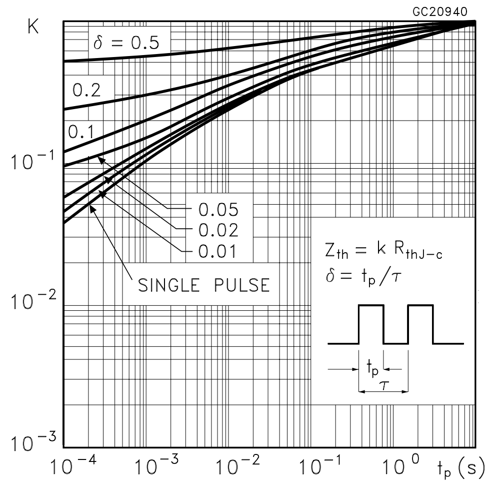


Figure 5: Output Characteristics

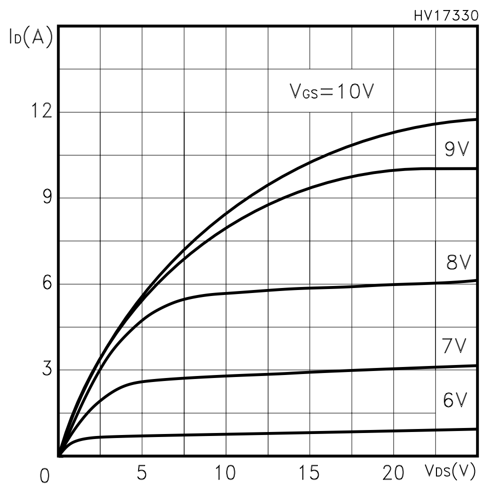


Figure 8: Transfer Characteristics

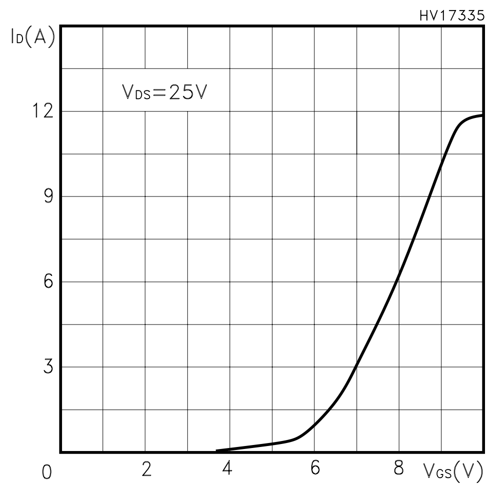


Figure 9: Transconductance

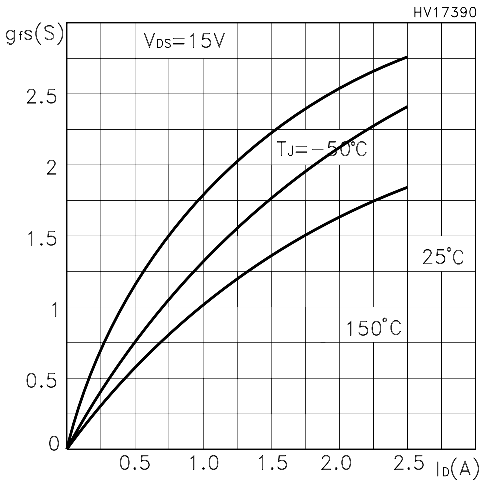


Figure 12: Static Drain-source On Resistance

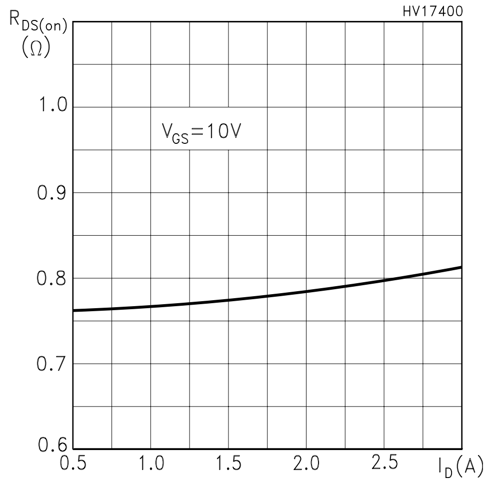


Figure 10: Gate Charge vs Gate-source Voltage

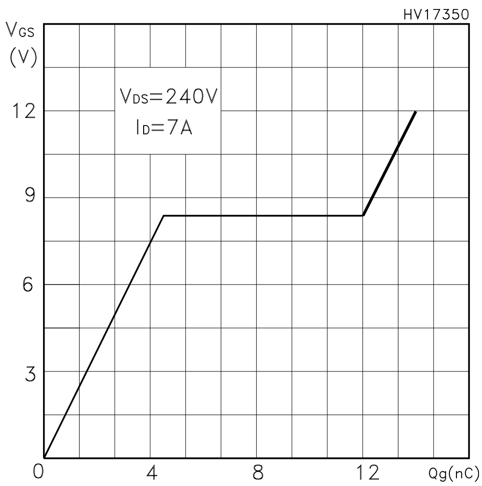


Figure 13: Capacitance Variations

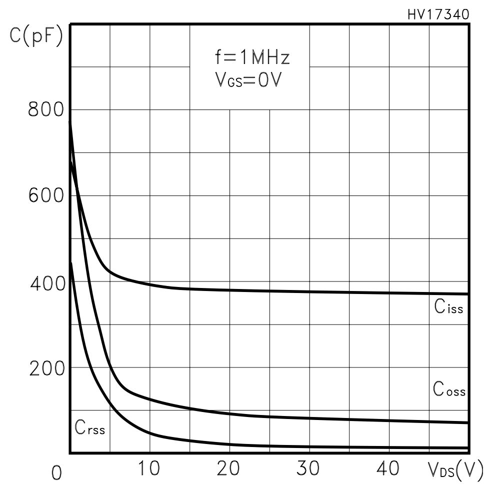


Figure 11: Normalized Gate Thereshold Voltage vs Temperature

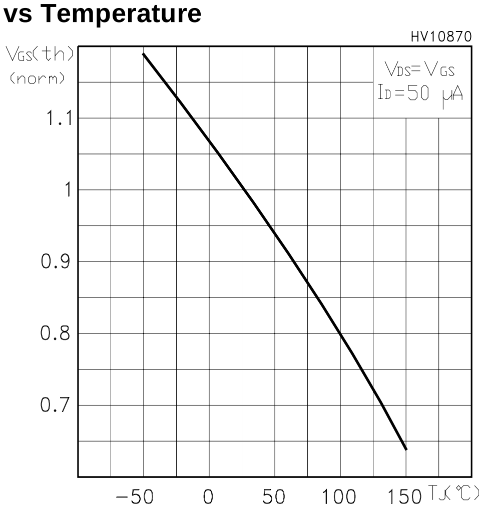


Figure 14: Normalized BVDSS vs Temperature

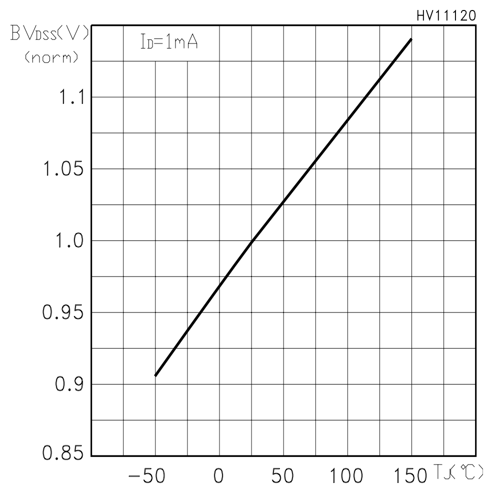


Figure 15: Normalized On Resistance vs TemperatureS

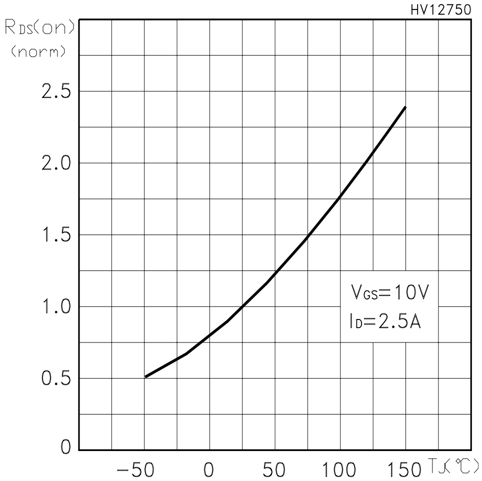


Figure 16: Source-Drain Diode Forward Characteristics

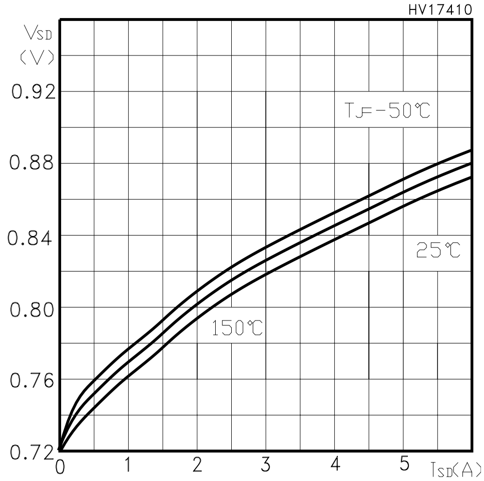


Figure 17: Unclamped Inductive Load Test Circuit

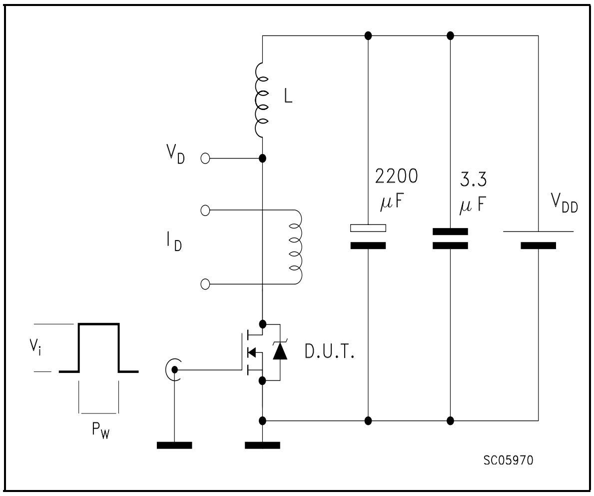


Figure 18: Switching Times Test Circuit For Resistive Load

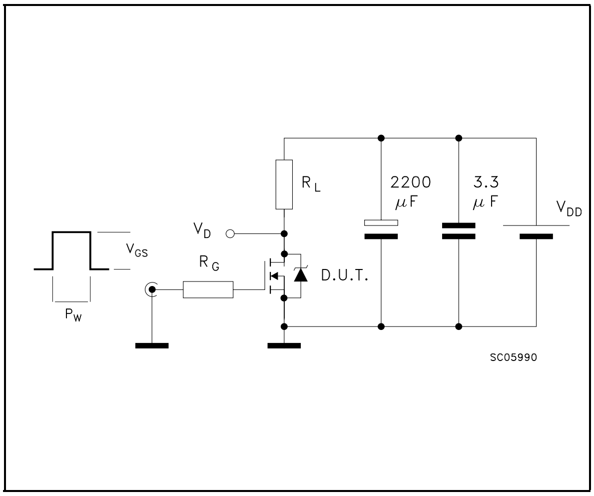


Figure 19: Test Circuit For Inductive Load Switching and Diode Recovery Times

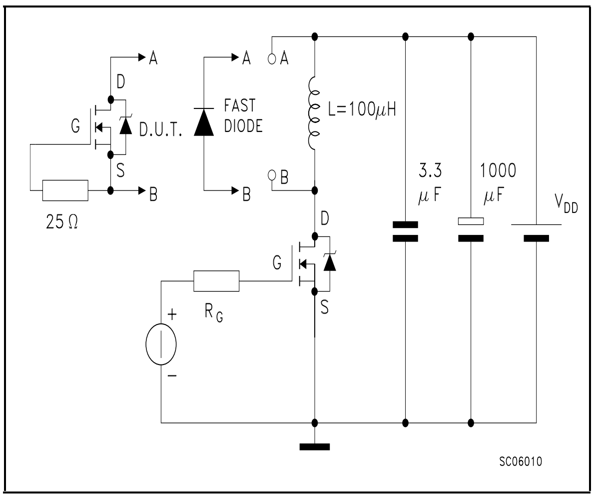


Figure 20: Unclamped Inductive Wafeform

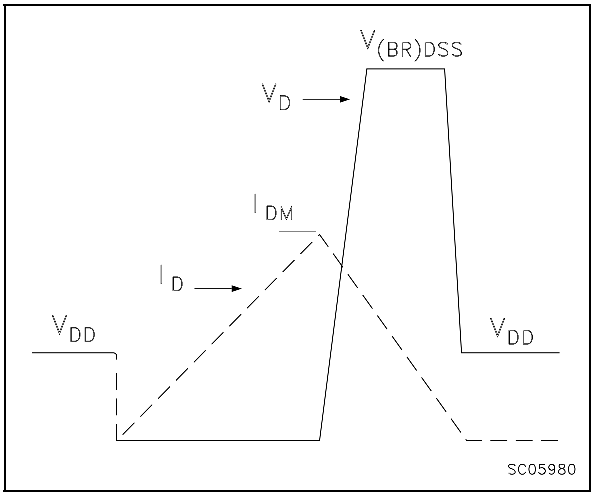
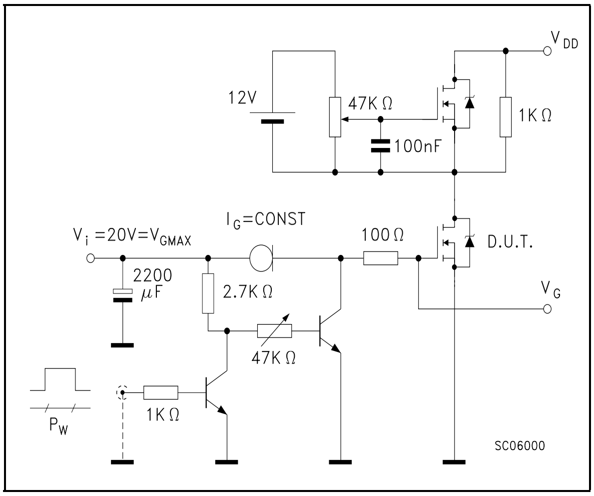


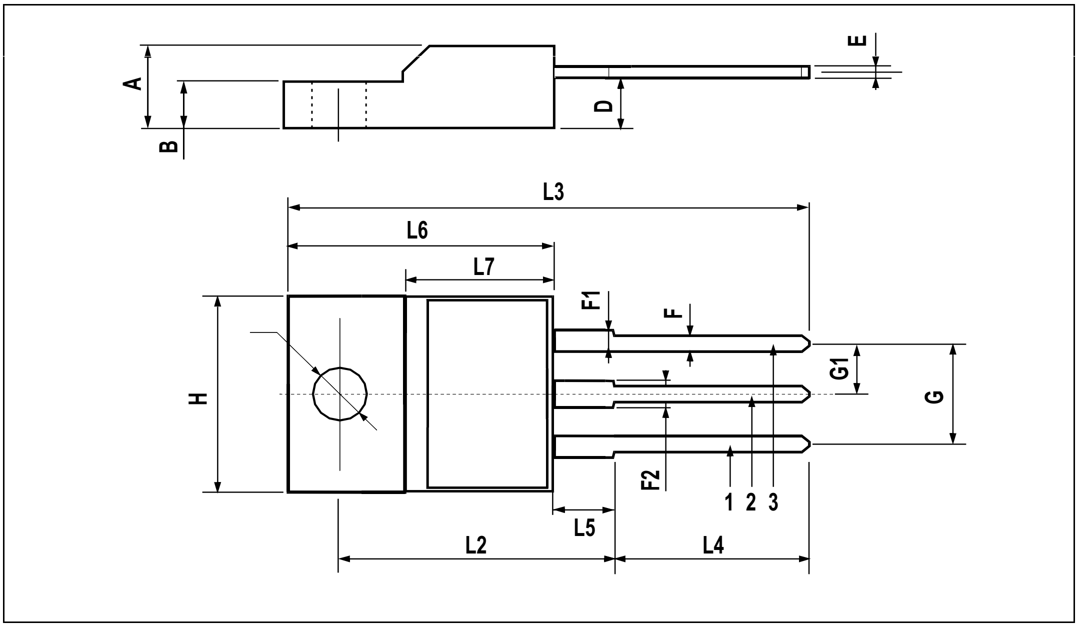
Figure 21: Gate Charge Test Circuit



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

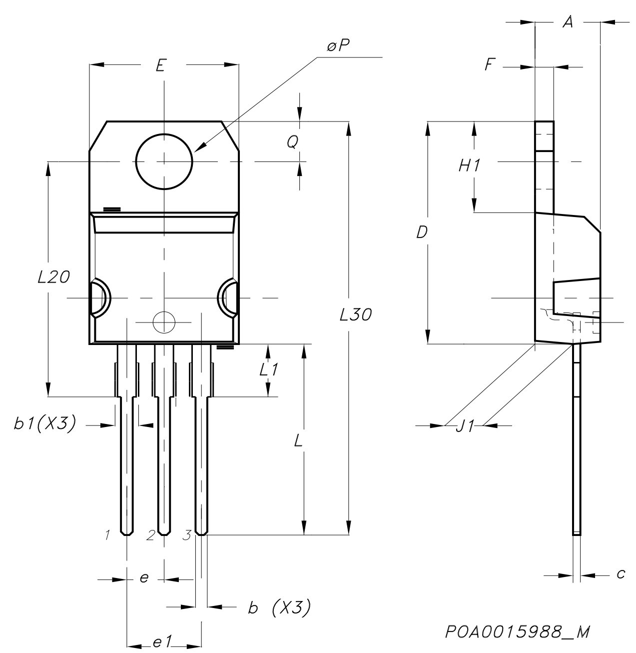


Table 10: Revision History

Date	Revision	Description of Changes
10-May-2005	1	New stylesheet
05-Sep-2005	2	Inserted Ecopack indication