RoHS ML Varistor Series

Size Table

Metric	EIA
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
4532	1812
5650	2220

Applications

- Suppression of Inductive Switching or Other Transient Events Such as EFT and Surge Voltage at the Circuit Board Level
- ESD Protection for Components Sensitive to IEC 61000-4-2, MIL-STD-883C Method 3015.7, and Other Industry Specifications (See Also the MLE or MLN Series)
- Provides On-Board Transient Voltage Protection for ICs and Transistors
- Used to Help Achieve Electromagnetic Compliance of End Products
- Replace Larger Surface Mount TVS Zeners in Many Applications

Description

The ML Series family of Transient Voltage Surge Suppression devices is based on the Littelfuse Multilayer fabrication technology. These components are designed to suppress a variety of transient events, including those specified in IEC 61000-4-2 or other standards used for Electromagnetic Compliance (EMC). The ML Series is typically applied to protect integrated circuits and other components at the circuit board level.

The wide operating voltage and energy range make the ML Series suitable for numerous applications on power supply, control and signal lines.

The ML Series is manufactured from semiconducting ceramics, and is supplied in a leadless, surface mount package. The ML Series is compatible with modern reflow and wave soldering procedures.

It can operate over a wider temperature range than zener diodes, and has a much smaller footprint than plastic-housed components.

Littelfuse Inc. manufactures other Multilayer Series products. See the MLE Series data sheet for ESD applications, MHS Series data sheet for high-speed ESD applications, the MLN for multiline protection and the AUML Series for automotive applications.

Features

- RoHS Compliant
- Leadless 0402, 0603, 0805, 1206 and 1210 Chip Sizes
- Multilayer Ceramic Construction Technology
- -55°C to +125°C Operating Temp. Range
- Operating Voltage Range $V_{M(DC)}$ = 5.5V to 120V
- Rated for Surge Current (8 x 20µs)
- Rated for Energy (10 x 1000µs)
- Inherent Bi-directional Clamping
- No Plastic or Epoxy Packaging Assures Better than 94V-0 Flammability Rating
- Standard Low Capacitance Types Available

Absolute Maximum Ratings

For ratings of individual members of a series, see device ratings and specifications table.

Continuous	ML Series	Units
Steady State Applied Voltage:		
DC Voltage Range ($V_{M(DC)}$)	3.5 to 120	V
AC Voltage Range ($V_{M(AC)RMS}$)	2.5 to 107	V
Transient:		
Non-Repetitive Surge Current, 8/20µs Waveform, (I_{TM})	4 to 500	A
Non-Repetitive Surge Energy, 10/1000µs Waveform, (W_{TM})	0.02 to 2.5	J
Operating Ambient Temperature Range (T_A)	-55 to + 125	°C
Storage Temperature Range (T_{STG})	-55 to + 150	°C
Temperature Coefficient (αV) of Clamping Voltage (V_C) at Specified Test Current	<0.01	%/°C

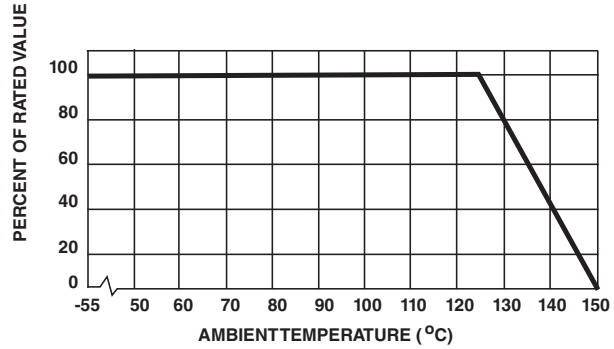
Device Ratings and Specifications

Part Number	Maximum Ratings (125°C)					Specifications (25°C)		
	Maximum Continuous Working Voltage		Maximum Non-repetitive Surge Current (8/20µs)	Maximum Non-repetitive Surge Energy (10/1000µs)	Maximum Clamping Voltage at 1A (or as Noted) (8/20µs)	Nominal Voltage at 1mA DC Test Current		Typical Capacitance at f = 1MHz
	$V_{M(DC)}$	$V_{M(AC)}$	I_{TM}	W_{TM}	V_C	$V_{N(DC)}$ Min	$V_{N(DC)}$ Max	C
	(V)	(V)	(A)	(J)	(V)	(V)	(V)	(pF)
V3.5MLA0603N[5]	3.5	2.5	30	0.100	13.0	3.7	7.0	1270
V3.5MLA0805N	3.5	2.5	120	0.300	13.0	3.7	7.0	2530
V3.5MLA0805LN	3.5	2.5	40	0.100	13.0	3.7	7.0	1380
V3.5MLA1206N	3.5	2.5	100	0.300	13.0	3.7	7.0	6000
V5.5MLA0402N	5.5	4.0	20	0.050	21.0	7.1	10.8	220
V5.5MLA0402LN	5.5	4.0	20	0.050	39.0	15.9	21.5	70
V5.5MLA0603N[5]	5.5	4.0	30	0.100	17.5	7.1	9.3	760
V5.5MLA0603LN[4]	5.5	4.0	30	0.100	17.5	7.1	9.3	450
V5.5MLA0805N	5.5	4.0	120	0.300	17.5	7.1	9.3	1840
V5.5MLA0805LN	5.5	4.0	40	0.100	17.5	7.1	9.3	990
V5.5MLA1206N	5.5	4.0	150	0.400	17.5	7.1	9.3	3500
V9MLA0402N	9.0	6.5	20	0.050	30.0	11.0	16.0	120
V9MLA0402LN	9.0	6.5	4	0.020	35.0	11.0	16.0	33
V9MLA0603N[5]	9.0	6.5	30	0.100	25.5	11.0	16.0	490
V9MLA0603LN[4]	9.0	6.5	30	0.100	25.5	11.0	16.0	360
V9MLA0805LN	9.0	6.5	40	0.100	25.5	11.0	16.0	520
V12MLA0805LN	12.0	9.0	40	0.100	29.0	14.0	18.5	410
V14MLA0402N	14.0	10.0	20	0.050	39.0	15.9	21.5	70
V14MLA0603N	14.0	10.0	30	0.100	34.5	15.9	21.5	180
V14MLA0805N	14.0	10.0	120	0.300	32.0	15.9	20.3	560
V14MLA0805LN	14.0	10.0	40	0.100	32.0	15.9	20.3	320
V14MLA1206N	14.0	10.0	150	0.400	32.0	15.9	20.3	1400
V18MLA0402N	18.0	14.0	20	0.050	50.0	22.0	28.0	40
V18MLA0603N	18.0	14.0	30	0.100	50.0	22.0	28.0	120
V18MLA0805N	18.0	14.0	120	0.300	44.0	22.0	28.0	520
V18MLA0805LN	18.0	14.0	40	0.100	44.0	22.0	28.0	290
V18MLA1206N	18.0	14.0	150	0.400	44.0	22.0	28.0	1270
V18MLA1210N	18.0	14.0	500	2.500	44.0 at 2.5A	22.0	28.0	1440
V26MLA0603N	26.0	20.0	30	0.100	60.0	31.0	38.0	110
V26MLA0805N	26.0	20.0	100	0.300	60.0	29.5	38.5	220
V26MLA0805LN	26.0	20.0	40	0.100	60.0	29.5	38.5	140
V26MLA1206N	26.0	20.0	150	0.600	60.0	29.5	38.5	600
V26MLA1210N	26.0	20.0	300	1.200	60.0 at 2.5A	29.5	38.5	1040
V30MLA0603N	30.0	25.0	30	0.100	74.0	37.0	46.0	90
V30MLA0805LN	30.0	25.0	30	0.100	72.0	37.0	46.0	90
V30MLA1210N	30.0	25.0	280	1.200	68.0 at 2.5A	35.0	43.0	1820
V30MLA1210LN	30.0	25.0	220	0.900	68.0 at 2.5A	35.0	43.0	1760
V33MLA1206N	33.0	26.0	180	0.800	75.0	38.0	49.0	500
V42MLA1206N	42.0	30.0	180	0.800	92.0	46.0	60.0	425
V48MLA1210N	48.0	40.0	250	1.200	105.0 at 2.5A	54.5	66.5	520
V48MLA1210LN	48.0	40.0	220	0.900	105.0 at 2.5A	54.5	66.5	500
V56MLA1206N	56.0	40.0	180	1.000	120.0	61.0	77.0	180
V60MLA1210N	60.0	50.0	250	1.500	130.0 at 2.5A	67.0	83.0	440
V68MLA1206N	68.0	50.0	180	1.000	140.0	76.0	90.0	100
V85MLA1210N	85.0	67.0	250	2.500	180.0 at 2.5A	95.0	115.0	260
V120MLA1210N	120.0	107.0	125	2.000	260.0 at 2.5A	135.0	165.0	80

NOTES:
1 L suffix is a low capacitance and energy version; Contact your Littelfuse Sales Representative for custom capacitance requirements.
2 Typical leakage at 25°C<25µA, maximum leakage 100µA at $V_{M(DC)}$; for 0402 size, typical leakage <5µA, maximum leakage <20µA at $V_{M(DC)}$.
3 Average power dissipation of transients for 0402, 0603, 0805, 1206 and 1210 sizes not to exceed 0.03W, 0.05W, 0.1W, 0.1W and 0.15W respectively.
4 Only Available in "R" packing option.
5 Only available in "H", "T"and "A" packing options.

Peak Current and Energy Derating Curve

When transients occur in rapid succession, the average power dissipation is the energy (watt-seconds) per pulse times the number of pulses per second. The power so developed must be within the specifications shown on the Device Ratings and Specifications table for the specific device. For applications exceeding 125°C ambient temperature, the peak surge current and energy ratings must be derated as shown below.



Peak Pulse Current Test Waveform for Clamping Voltage

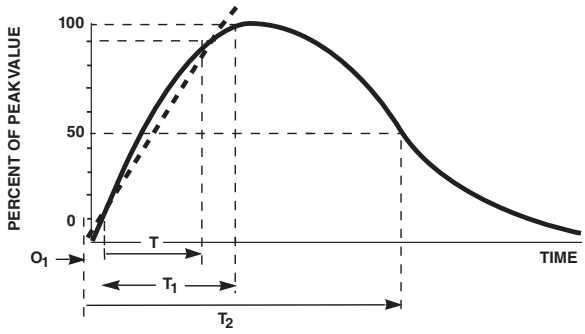
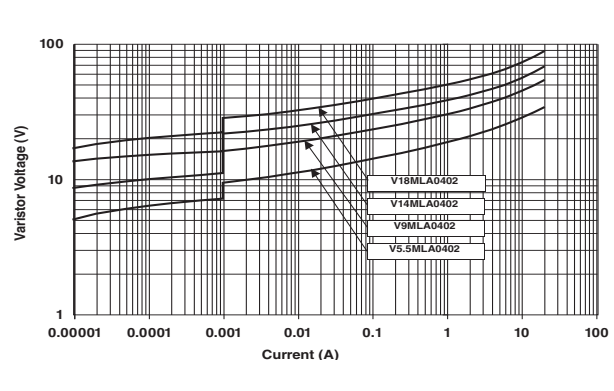


FIGURE 2. PEAK PULSE CURRENT TES FOR CLAMPING VOLTAGE

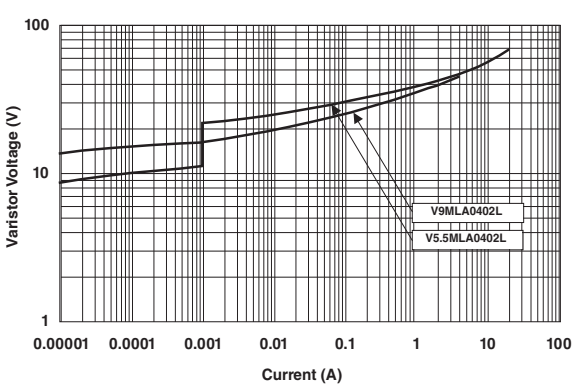
O_1 = VIRTUAL ORIGIN OF WAVE
t = TIME FROM 10% TO 90% OF PEAK
t_1 = VIRTUAL FRONT TIME = 1.25 x t
t_2 = VIRTUAL TIME TO HALF VALUE (IMPULSE DURATION)

EXAMPLE:
FOR AN 8/20 s CURRENT WAVEFORM

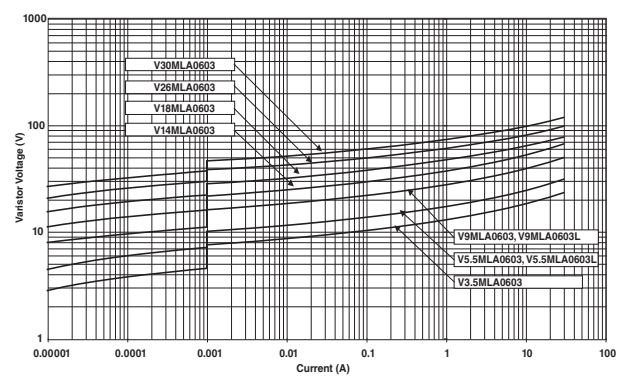
Limit V-I Characteristic for V5.5MLA0402 to V18MLA0402



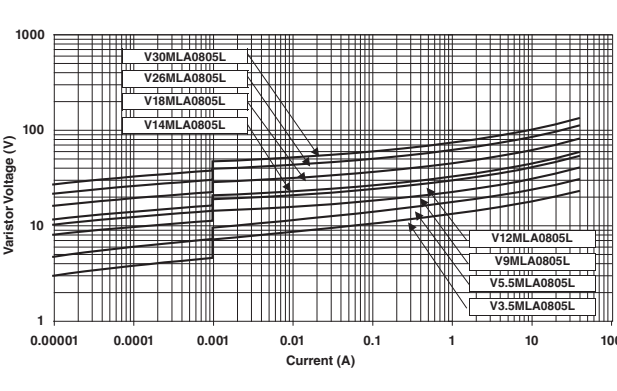
Limit V-I Characteristic for V9MLA0402L



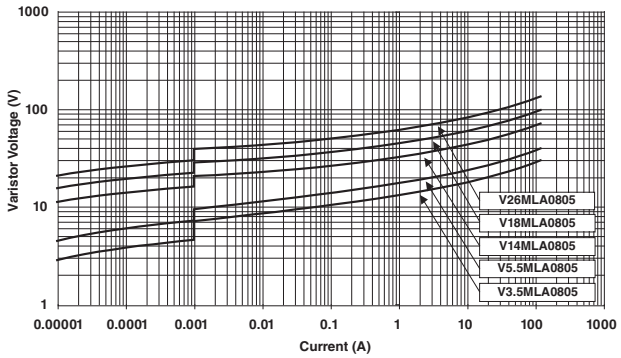
Limit V-I Characteristic for V3.5MLA0603 to V30MLA0603



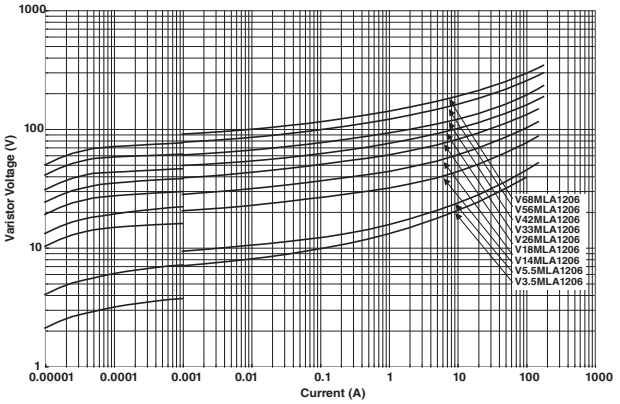
Limit V-I Characteristic for V3.5MLA0805L to V30MLA0805L



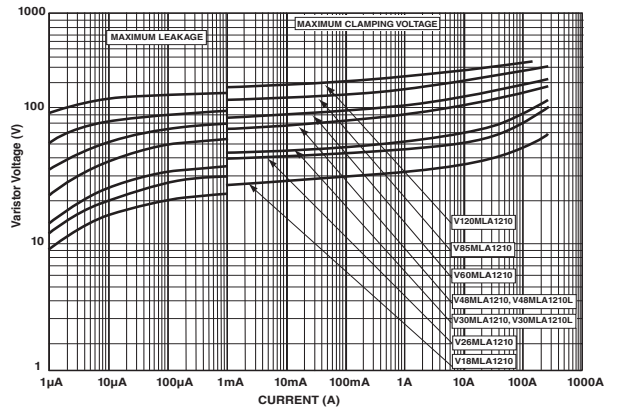
Limit V-I Characteristic for V3.5MLA0805 to V26MLA0805



Limit V-I Characteristic for V3.5MLA1206 to V68MLA1206



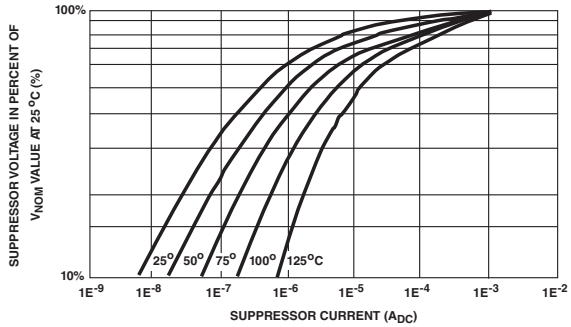
Limit V-I Characteristic for V18MLA1210 to V120MLA1210



Device Characteristics

At low current levels, the V-I curve of the multilayer transient voltage suppressor approaches a linear (ohmic) relationship and shows a temperature dependent effect. At or below the maximum working voltage, the suppressor is in a high resistance modex (approaching $10^6\Omega$ at its maximum rated working voltage). Leakage currents at maximum rated voltage are below 100µA, typically 25µA; for 0402 size below 20µA, typically 5µA.

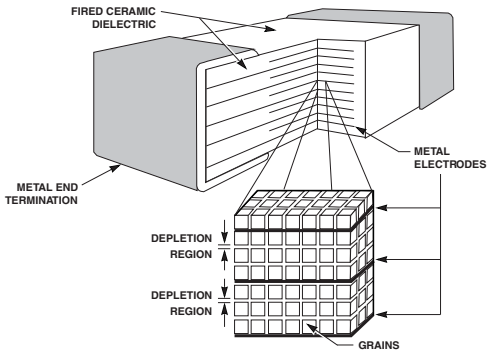
Typical Temperature Dependance of the Haracteristic Curve in the Leakage Region



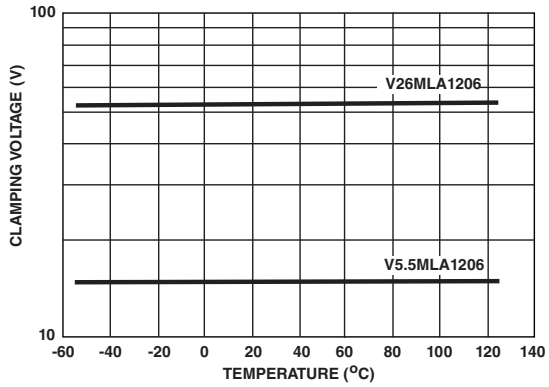
Speed of Response

The Multilayer Suppressor is a leadless device. Its response time is not limited by the parasitic lead inductances found in other surface mount packages. The response time of the Zinc Oxide dielectric material is less than 1 nanosecond and the ML can clamp very fast dV/dT events such as ESD. Additionally, in "real world" applications, the associated circuit wiring is often the greatest factor effecting speed of response. Therefore, transient suppressor placement within a circuit can be considered important in certain instances.

Multilayer Internal Construction



Clamping Voltage Over Temperature (V_C at 10A)

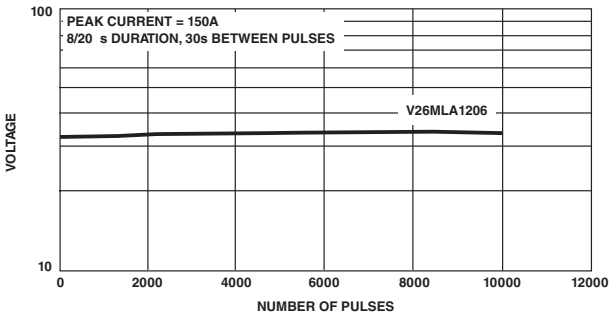


Energy Absorption/Peak Current Capability

Energy dissipated within the ML is calculated by multiplying the clamping voltage, transient current and transient duration. An important advantage of the multilayer is its interdigitated electrode construction within the mass of dielectric material. This results in excellent current distribution and the peak temperature per energy absorbed is very low. The matrix of semiconducting grains combine to absorb and distribute transient energy (heat) (see Speed of Response). This dramatically reduces peak temperature; thermal stresses and enhances device reliability.

As a measure of the device capability in energy and peak current handling, the V26MLA1206A part was tested with multiple pulses at its peak current rating (150A, 8/20µs). At the end of the test, 10,000 pulses later, the device voltage characteristics are still well within specification.

Repetitive Pulse Capability



Lead (Pb) Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are IR Re-flow & Wave soldering. Typical profiles are shown on the right.

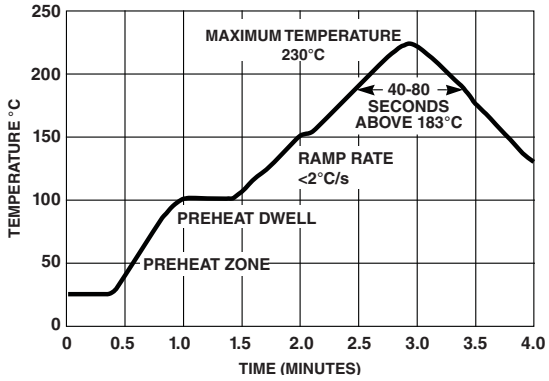
The recommended solder for the ML suppressor is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb) or 63/37 (Sn/Pb). Littelfuse also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

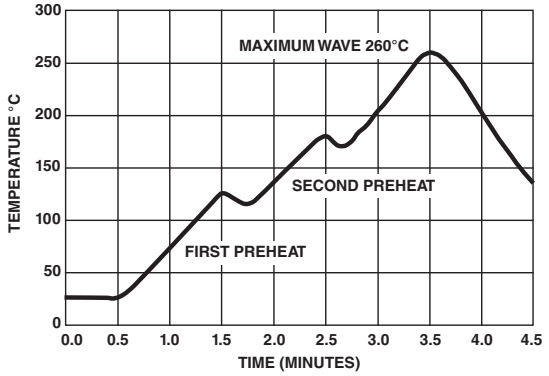
When using a reflow process, care should be taken to ensure that the ML chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solderís peak temperature is essential to minimize thermal shock.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to cool gradually to less than 50˚C before cleaning.

Reflow Solder Profile



Wave Solder Profile



Lead-free (Pb-free) Soldering Recommendations

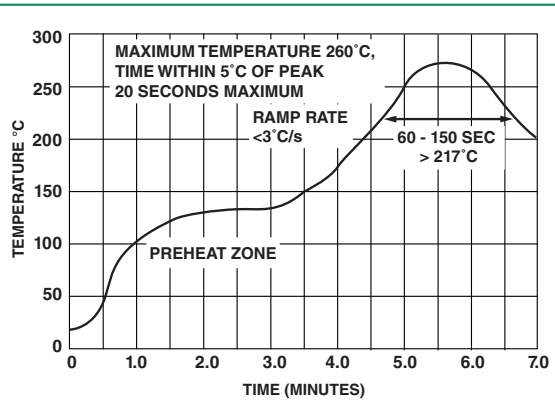
Littelfuse offers the Nickel-Barrier termination finish for the optimum Pb-free solder performance.

The preferred solder is 96.5/3.0/0.5 (SnAgCu) with an RMA flux, but there is a wide selection of pastes & fluxes available with which the nickel barrier parts should be compatible.

The reflow profile must be constrained by the maximums in the Lead-free Reflow Profile. For Pb-free Wave soldering, the Wave Solder Profile still applies.

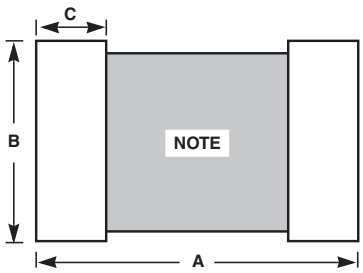
Note: the Pb-free paste, flux & profile were used for evaluation purposes by Littelfuse, based upon industry standards & practices. There are multiple choices of all three available, it is advised that the customer explores the optimum combination for their process as processes vary considerably from site to site.

Lead-free Re-flow Solder Profile



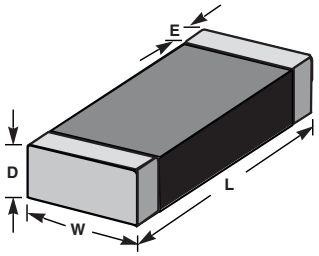
Dimensions

PAD LAYOUT DIMENSIONS



NOTE : Avoid metal runs in this area, parts not recommended for use in applications using Silver Epoxy Paste.

CHIP LAYOUT DIMENSIONS



Dimension	1210 Size Device		1206 Size Device		0805 Size Device		0603 Size Device		0402 Size Device	
	IN	MM	IN	MM	IN	MM	IN	MM	IN	MM
A	0.160	4.06	0.160	4.06	0.120	3.05	0.100	2.54	0.067	1.70
B	0.100	2.54	0.065	1.65	0.050	1.27	0.030	0.76	0.020	0.51
C	0.040	1.02	0.040	1.02	0.040	1.02	0.035	0.89	0.024	0.61
D Max.	0.113	2.87	0.071	1.80	0.043	1.10	0.040	1.00	0.024	0.90
E	0.020 ±0.010	0.50 ±0.25	0.020 ±0.010	0.50 ±0.25	0.020 ± 0.010	0.50 ± 0.25	0.015 ±0.008	0.4 ±0.20	0.010 ±0.006	0.25 ±0.15
L	0.125 ±0.012	3.20 ±0.30	0.125 ±0.012	3.20 ±0.30	0.079 ±0.008	2.01 ±0.20	0.063 ±0.006	1.6 ±0.15	0.039 ±0.004	1.00 ±0.10
W	0.100 ±0.012	2.54 ±0.30	0.060 ±0.011	1.60 ±0.28	0.049 ±0.008	1.25 ±0.20	0.032 ±0.060	0.8 ±0.15	0.020 ±0.004	0.50 ±0.10

Part Numbering System

V 18 MLA 1206 X X X

DEVICE FAMILY
Littelfuse TVSS Device

MAXIMUM DC WORKING VOLTAGE

MULTILAYER SERIES DESIGNATOR

DEVICE SIZE:
i.e., 120 mil x 60 mil
(3mm x 1.5mm)

PACKING OPTIONS
T: 13in (330mm) Diameter Reel, Plastic Carrier Tape
H: 7in (178mm) Diameter Reel, Plastic Carrier Tape
R: 7in (178mm) Diameter Reel, Paper Carrier Tape

END TERMINATION OPTION
N: Nickel Barrier (Ni/Sn)

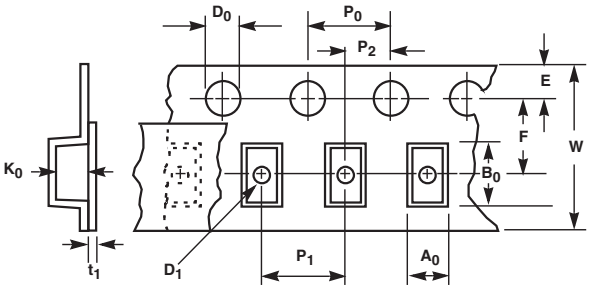
CAPACITANCE OPTION
No Letter: Standard
L: Low Capacitance Version

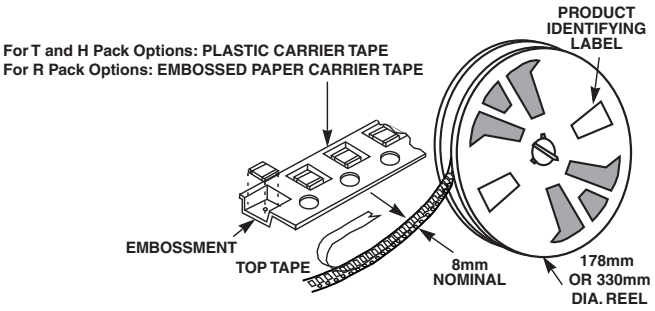
Packaging

Device Size	13" Inch Reel ("T" Option)	7" Inch Reel ("H" Option)	7" Inch Reel ("R" Option)	Bulk Pack ("A" Option)
1210	8,000	2,000	N/A	2,000
1206	10,000	2,500	N/A	2,500
0805	10,000	2,500	N/A	2,500
0603	10,000	2,500	4,000	2,500
0402	N/A	N/A	10,000	N/A

*NOTES:
1 V120MLA1210 standard shipping quantities are 1000 pieces per reel for "H" option and 4000 pieces per reel for "T" option.
2 V3.5 MLA0603, V5.5MLA0603 and V9MLA0603 only available in "H", "T"and "A" packing options.

Tape and Reel Specifications





Symbol	Description	Dimensions in Millimeters	
		0402 Size	0603, 0805, 1206 & 1210 Sizes
A_0	Width of Cavity	Dependent on Chip Size to Minimize Rotation.	
B_0	Length of Cavity	Dependent on Chip Size to Minimize Rotation.	
K_0	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.	
W	Width of Tape	8 ±0.2	8 ±0.3
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ±0.05	3.5 ±0.05
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ±0.1	1.75 ±0.1
P_1	Distance Between Cavity Centers	2±0.05	4 ±0.1
P_2	Axial Drive Distance Between Drive Hole Centers & Cavity Centers	2 ±0.1	2 ±0.1
P_0	Axial Drive Distance Between Drive Hole Centers	4 ±0.1	4 ±0.1
D_0	Drive Hole Diameter	1.55 ±0.05	1.55 ±0.05
D_1	Diameter of Cavity Piercing	N/A	1.05 ±0.05
T_1	Top Tape Thickness	0.1 Max	0.1 Max

NOTES:
- Conforms to EIA-481-1, Revision A
- Can be supplied to IEC publication 286-3