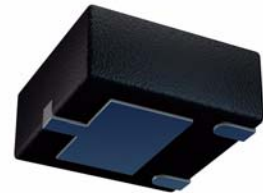


ZXMN2F34MA

20V N-channel enhancement mode MOSFET in DFN322

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.060 @ $V_{GS} = 4.5V$	8.5
	0.120 @ $V_{GS} = 2.5V$	

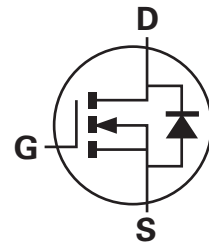


Description

This new generation Trench MOSFET from Zetex features low on-resistance achievable with low (2.5V) gate drive. The 2mm x 2mm DFN package provides superior thermal performance versus alternative leaded devices

Features

- Low on-resistance
- Superior thermal performance (versus to SOT23)
- 2.5V gate drive capability
- DFN 2x2 package

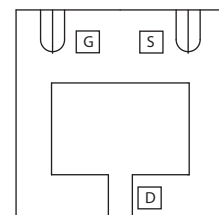


Applications

- Buck/Boost DC-DC Converters
- Motor Control
- LED Lighting

Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN2F34MATA	7	8	3,000



Device marking

1M4

ZXMN2F34MA

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	20	V
Gate source voltage	V_{GS}	± 12	V
Continuous Drain Current @ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(b)}$	I_D	5.1	A
@ $V_{GS}=4.5$; $T_A=70^\circ\text{C}^{(b)}$		4.1	A
@ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(a)}$		4.0	A
@ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(d)}$		8.5	A
Pulsed drain current ^(c)	I_{DM}	19	A
Continuous source current (body diode) ^(b)	I_S	3.1	A
Pulsed source current (body diode) ^(c)	I_{SM}	19	A
Power dissipation at $T_A=25^\circ\text{C}^{(a)}$	P_D	1.35	W
Linear derating factor		10.8	mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(b)}$	P_D	2.2	W
Linear derating factor		17.8	mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(d)}$	P_D	6.6	W
Linear derating factor		52.9	mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	°C

Thermal resistance

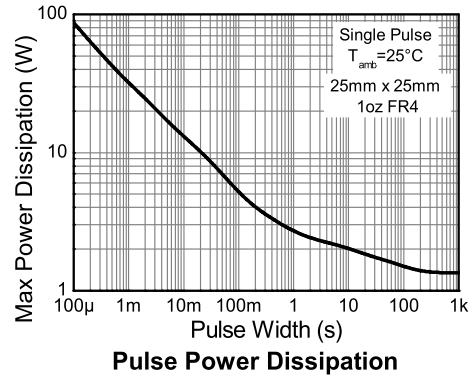
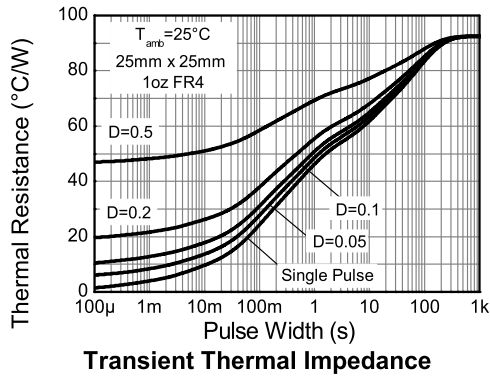
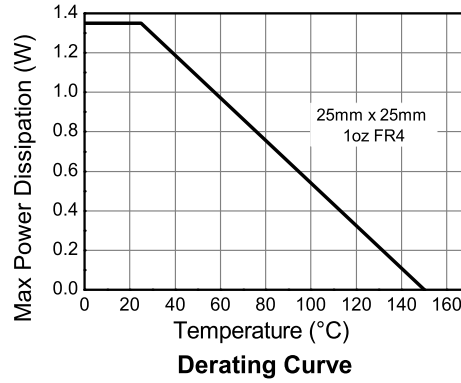
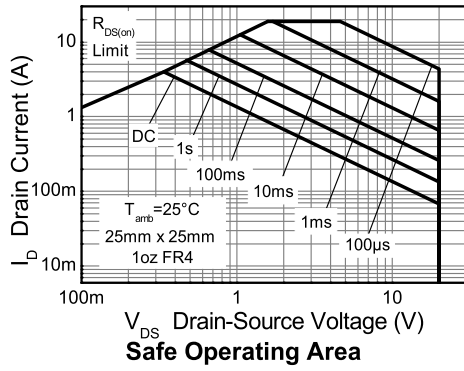
Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	92.5	°C/W
Junction to ambient ^(b)	$R_{\theta JA}$	56	°C/W
Junction to lead ^(d)	$R_{\theta JL}$	18.9	°C/W

NOTES:

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 5$ sec.
- (c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.
- (d) Thermal resistance from junction to solder-point (at end of drain lead).

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Thermal characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	20			V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body leakage	I_{GSS}			100	nA	$V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source threshold voltage	$V_{GS(th)}$	0.5	0.8	1.5	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.060 0.120	Ω Ω	$V_{GS} = 4.5\text{V}$, $I_D = 2.5\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 1.0\text{A}$
Forward transconductance(*)†	g_{fs}		7.5		S	$V_{DS} = 10\text{V}$, $I_D = 2.5\text{A}$
Dynamic †						
Input capacitance	C_{iss}		277		pF	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output capacitance	C_{oss}		65		pF	
Reverse transfer capacitance	C_{rss}		35		pF	
Switching ‡†						
Turn-on-delay time	$t_{d(on)}$		2.65		ns	$V_{DD} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 1\text{A}$ $R_G \approx 6.0\Omega$
Rise time	t_r		4.2		ns	
Turn-off delay time	$t_{d(off)}$		9.9		ns	
Fall time	t_f		5.1		ns	
Total gate charge	Q_g		2.8		nC	$V_{DS} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 2.5\text{A}$
Gate-Source charge	Q_{gs}		0.61		nC	
Gate Drain charge	Q_{gd}		0.63		nC	
Source-drain diode						
Diode forward voltage(*)	V_{SD}		0.73	1.2	V	$I_S = 1.25\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time†	t_{rr}		6.5		ns	$T_j = 25^{\circ}\text{C}$, $I_F = 1.65\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge†	Q_{rr}		1.4		nC	

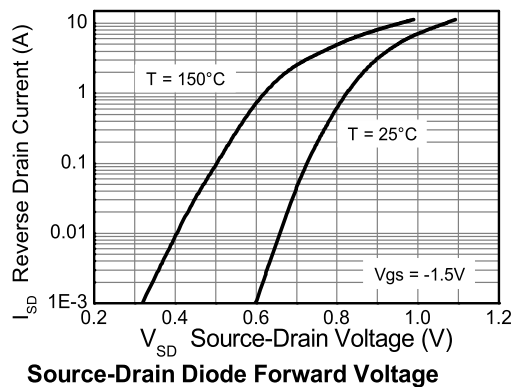
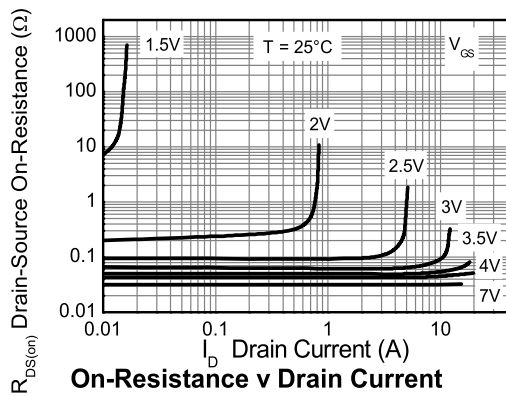
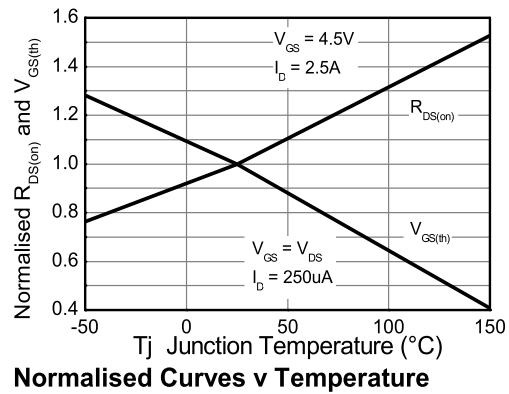
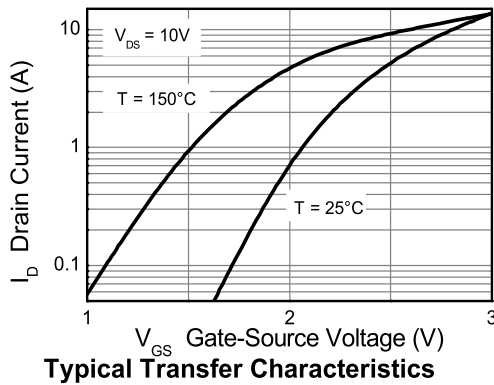
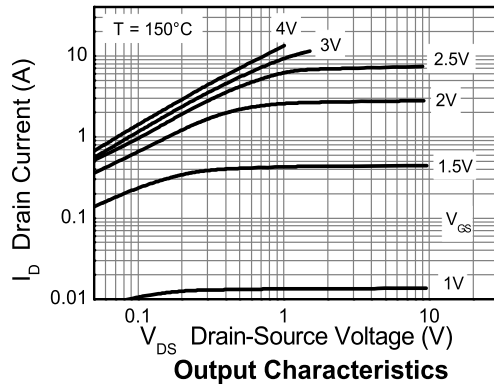
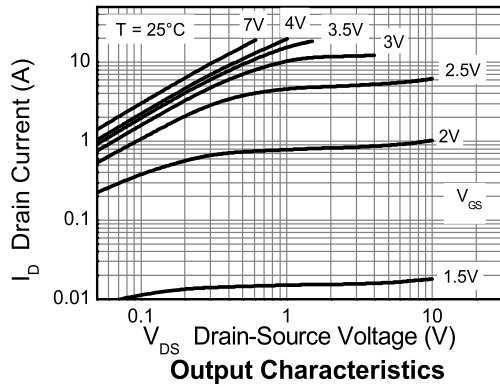
NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

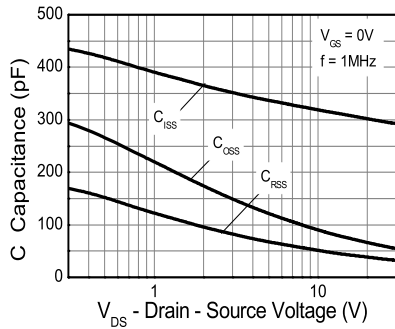
† For design aid only, not subject to production testing.

‡ Switching characteristics are independent of operating junction temperature.

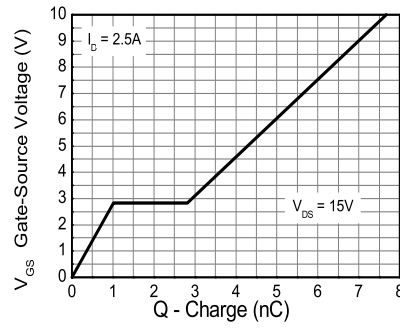
Typical characteristics



Typical characteristics

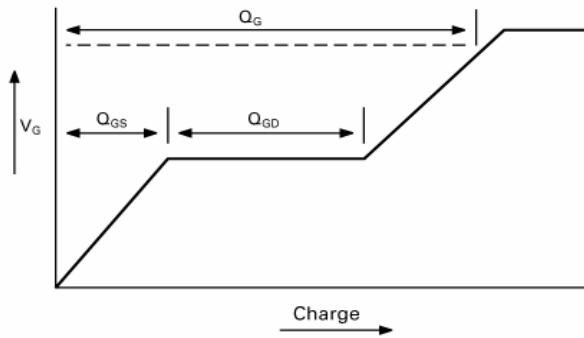


Capacitance v Drain-Source Voltage

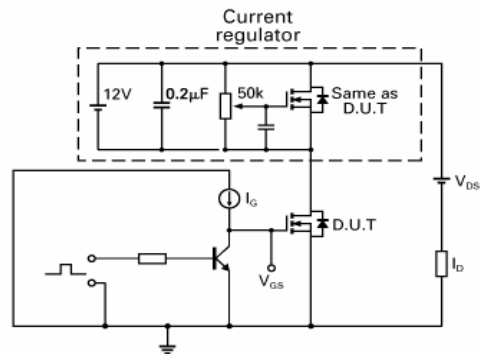


Gate-Source Voltage v Gate Charge

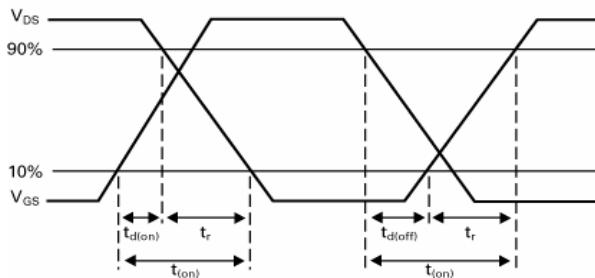
Test circuits



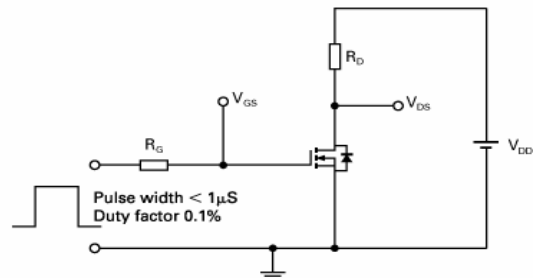
Basic gate charge waveform



Gate charge test circuit



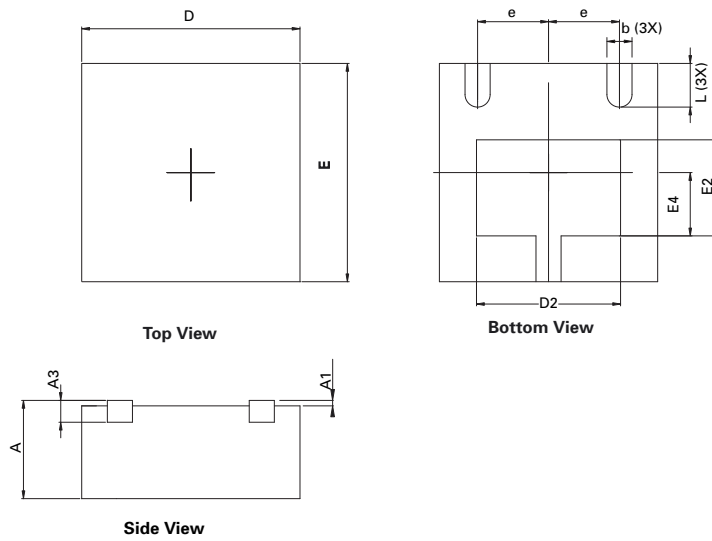
Switching time waveforms



Switching time test circuit

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Package outline - DFN322



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.80	1.00	0.0315	0.0393	D2	1.22	1.42	0.0480	0.0559
A1		0.05		0.002	e	0.65 BSC.		0.02559 BSC	
A3	0.153	0.253	0.0060	0.0099	E	1.900	2.100	0.0748	0.0826
b	0.180	0.300	0.0071	0.0118	E2	0.780	0.990	0.0307	0.0389
D	1.900	2.100	0.0748	0.0826	E4	0.480	0.680	0.0189	0.0267
					L	0.300	0.500	0.0118	0.0196

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

ZXMN2F34MA

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