SN74ALVCH16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES025E-JULY 1995-REVISED OCTOBER 2004

FEATURES

- Member of the Texas Instruments Widebus™
 Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

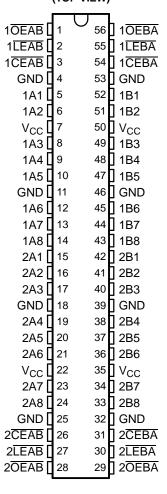
DESCRIPTION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V $V_{\rm CC}$ operation.

The SN74ALVCH16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using CEBA, LEBA, and OEBA.

DGG OR DL PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

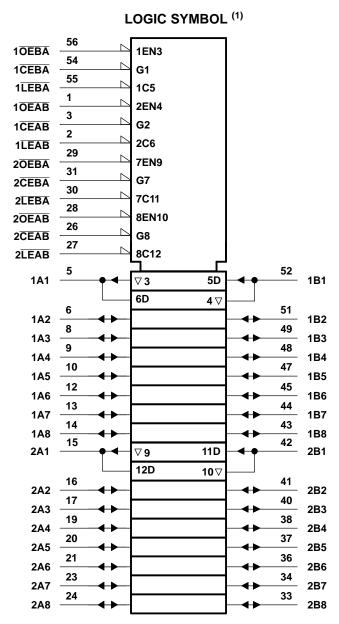
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16543 is characterized for operation from -40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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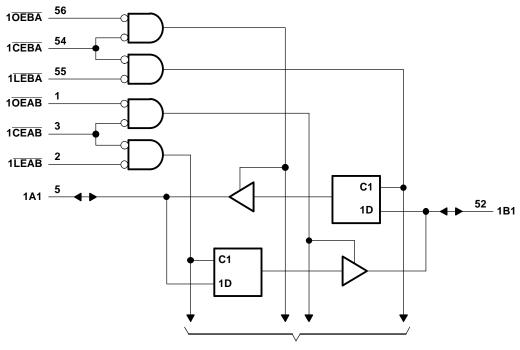




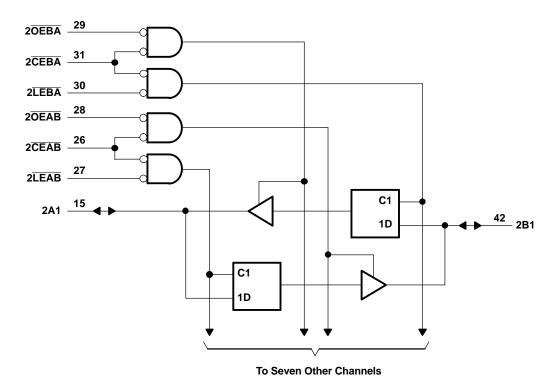
(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



LOGIC DIAGRAM (POSITIVE LOGIC)



To Seven Other Channels



3

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FUNCTION TABLE⁽¹⁾ (each 8-bit section)

	INPUTS								
CEAB	LEAB	OEAB	Α	В					
Н	Χ	Χ	Χ	Z					
X	Χ	Н	Χ	Z					
L	Н	L	Χ	B ₀ ⁽²⁾					
L	L	L	L	L					
L	L	L	Н	Н					

- (1) A-to-B data flow is shown; B-to-A flow control is the same, except that it uses CEBA, LEBA, and OEBA.
- Output level before the indicated steady-state input conditions were established

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
.,	land to alternation	Except I/O ports ⁽²⁾	-0.5	4.6	W
VI	Input voltage range	I/O ports (2) (3)	-0.5	$V_{CC} + 0.5$	V
Vo	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GND			±100	mA
0	Deckers thermal impedance (4)	DGG package		81	°C/W
θ_{JA}	Package thermal impedance ⁽⁴⁾	DL package		74	-C/VV
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.



WITH 3-STATE OUTPUTS

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RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
	High level output ourrent	V _{CC} = 2.3 V		-12	mA
I _{OH}	High-level output current	V _{CC} = 2.7 V		-12	IIIA
		V _{CC} = 3 V		-24	
		V _{CC} = 1.65 V		4	
	Low lovel output ourrent	V _{CC} = 2.3 V		12	A
I _{OL}	I _{OL} Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST C	ONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} - 0.2				
		I _{OH} = -4 mA		1.65 V	1.2				
		I _{OH} = -6 mA		2.3 V	2				
V_{OH}				2.3 V	1.7			V	
		I _{OH} = -12 mA		2.7 V	2.2				
				3 V	2.4				
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 4 mA		1.65 V			0.45		
\/		I _{OL} = 6 mA		2.3 V			0.4	\/	
V _{OL}		L - 12 mΔ	2.3				0.7	V	
		I _{OL} = 12 mA		2.7 V			0.4		
		I _{OL} = 24 mA		3 V			0.55		
I		$V_I = V_{CC}$ or GND		3.6 V			±5	μΑ	
		V _I = 0.58 V		1.65 V	25				
		V _I = 1.07 V		1.65 V	-25				
		$V_1 = 0.7 \ V$		2.3 V	45				
I _{I(hold)}		V _I = 1.7 V		2.3 V	-45			μΑ	
		$V_{I} = 0.8 \text{ V}$		3 V	75				
		V _I = 2 V		3 V	-75				
		$V_I = 0$ to 3.6 $V^{(2)}$		3.6 V			±500		
$I_{OZ}^{(3)}$		$V_O = V_{CC}$ or GND		3.6 V			±10	μΑ	
I_{CC}		$V_I = V_{CC}$ or GND,	$I_{O} = 0$	3.6 V			40	μΑ	
ΔI_{CC}		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		3.5		pF	
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		8.5		pF	

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

				V _{CC} = 1.8 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE or CE low				3.3		3.3		3.3		ns
t _{su}	Setup time	Data before <u>LE</u> ↑ or <u>CE</u> ↑	(1)		1.2		1.5		1.2		ns
t _h	Hold time	Data after LE↑ or CE↑	(1)		1.2		0.8		1.3		ns

⁽¹⁾ This information was not available at the time of publication.

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to

⁽³⁾ For I/O ports, the parameter $I_{\mbox{\scriptsize OZ}}$ includes the input leakage current.





SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	ARAMETER FROM TO		V _{CC} = 1.8 V	V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT	
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX		
4	A or B	B or A	(1)	1	5.1		4.8	1	4.3	20	
t _{pd}	ĪĒ	A or B	(1)	1	6.5		6.2	1.1	5	ns	
t _{en}	CE	A or B	(1)	1	7.2		6.9	1	5.6	ns	
t _{dis}	CE	A or B	(1)	1.3	6.1		6.2	1.5	5.1	ns	
t _{en}	ŌĒ	A or B	(1)	1	6.8		6.3	1	5.3	ns	
t _{dis}	ŌĒ	A or B	(1)	1	5.7		4.8	1.1	4.6	ns	

⁽¹⁾ This information was not available at the time of publication.

OPERATING CHARACTERISTICS

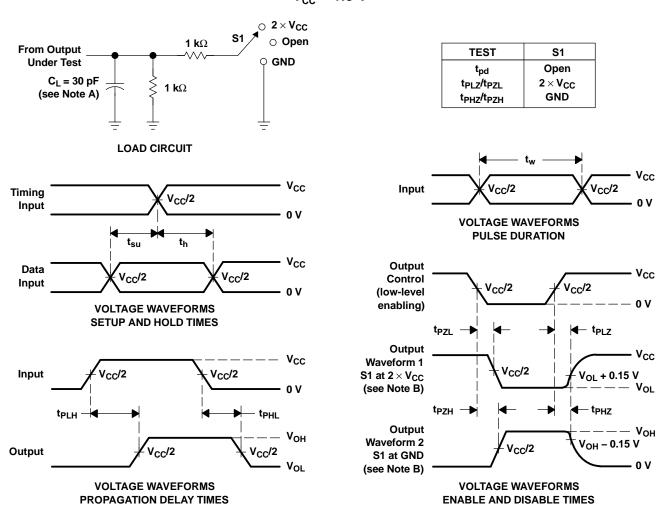
 $T_A = 25^{\circ}C$

	PARAME	TER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
0	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	(1)	54	64	ρF
C _{pd}	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	(1)	6	7	рг

⁽¹⁾ This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8 \text{ V}$

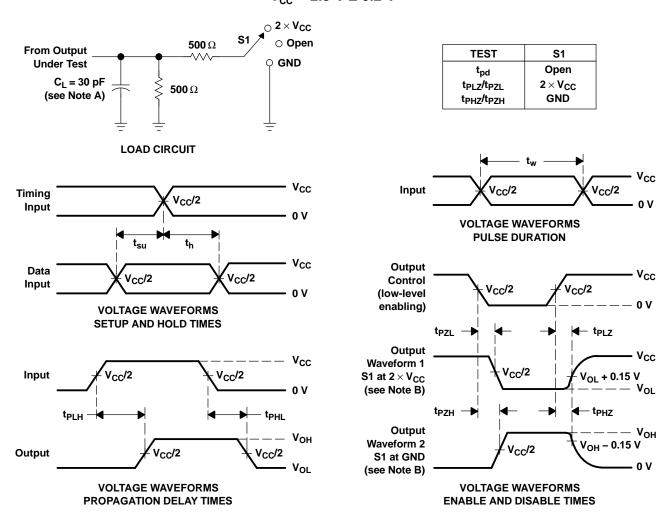


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z $_{O}$ = 50 $\Omega,\,t_{f}$ \leq 2 ns. t_{f} \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PL7} and t_{PH7} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION $V_{\rm CC}$ = 2.5 V \pm 0.2 V



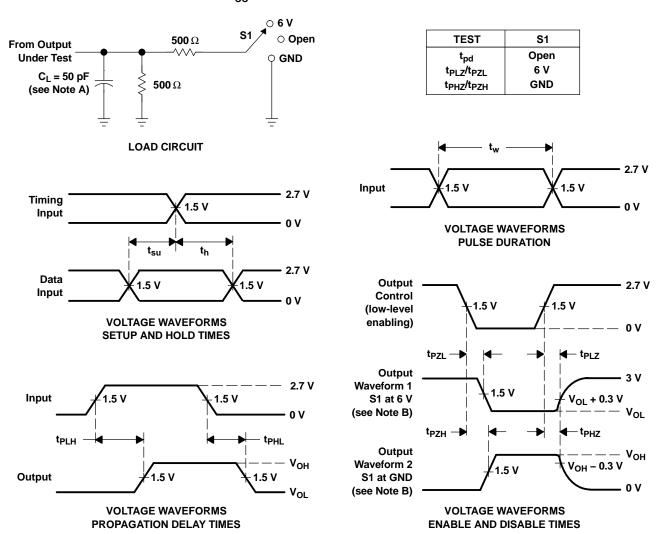
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2 ns, $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms





27-Sep-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16543DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16543DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16543DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16543DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16543DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16543DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16543DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16543DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16543DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

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