

CY54FCT541T, CY74FCT541T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCCS072 – OCTOBER 2001

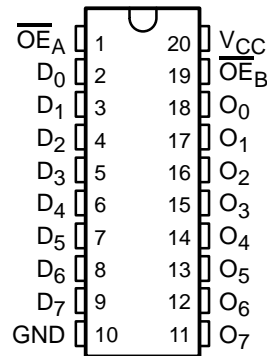
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT541T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT541T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

description

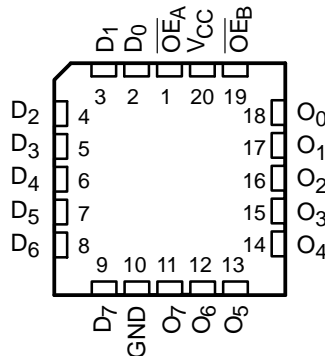
The 'FCT541T noninverting buffers/line drivers can be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar-logic counterparts, while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT541T . . . D PACKAGE
CY74FCT541T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT541T . . . L PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT541CTQCT	FCT541C
	SOIC – SO	Tube	4.1	CY74FCT541CTSOC	FCT541C
		Tape and reel	4.1	CY74FCT541CTSOCT	
	DIP – P	Tube	4.8	CY74FCT541ATPC	CY74FCT541ATPC
	QSOP – Q	Tape and reel	4.8	CY74FCT541ATQCT	FCT541A
	SOIC – SO	Tube	4.8	CY74FCT541ATSOC	FCT541A
		Tape and reel	4.8	CY74FCT541ATSOCT	
	SOIC – SO	Tube	8	CY74FCT541TSOC	FCT541
Tape and reel		8	CY74FCT541TSOCT		
-55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT541CTDMB	
	CDIP – D	Tube	8	CY54FCT541TDMB	
	LCC – L	Tube	8	CY54FCT541TLMB	

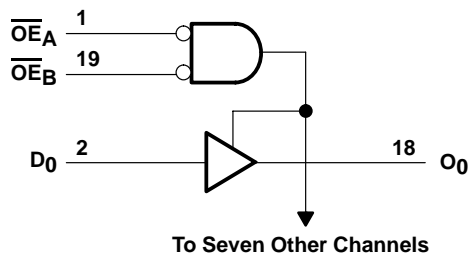
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}_A	\overline{OE}_B	D	O
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

logic diagram (positive logic)



CY54FCT541T, CY74FCT541T

8-BIT BUFFERS/LINE DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT541T		CY74FCT541T		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2			V	
	V _{CC} = 4.75 V, I _{IN} = -18 mA				-0.7 -1.2		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3			V	
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2		
		I _{OH} = -15 mA			2.4		3.3
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.3	0.55			V	
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3 0.55		
V _{hys}	All inputs	0.2			0.2	V	
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5		μA	
	V _{CC} = 5.25 V, V _{IN} = V _{CC}				5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1		μA	
	V _{CC} = 5.25 V, V _{IN} = 2.7 V				±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1		μA	
	V _{CC} = 5.25 V, V _{IN} = 0.5 V				±1		
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V			10		μA	
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V				10		
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V			-10		μA	
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V				-10		
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225		mA	
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60 -120 -225		
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1		μA	
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V		0.1	0.2		mA	
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1 0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open		0.5	2		mA	
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5 2		
I _{CCD} ¶	V _{CC} = 5.5 V, 50% duty cycle, Outputs open, One bit switching at f ₁ = 10 MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ and $\overline{OE}_B = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V		0.06	0.12		mA/MHz	
	V _{CC} = 5.25 V, 50% duty cycle, Outputs open, One bit switching at f ₁ = 10 MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ and $\overline{OE}_B = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				0.06 0.12		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT541T		CY74FCT541T		UNIT
				MIN	TYP†	MAX	MIN	
I _C #	V _{CC} = 5.5 V, Outputs open, OE _A = OE _B = GND or OE _A = GND and OE _B = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.7	1.4			mA
			V _{IN} = 3.4 V or GND	1	2.4			
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	1.3	2.6			
			V _{IN} = 3.4 V or GND	3.3	10.6			
	V _{CC} = 5.25 V, Outputs open, OE _A = OE _B = GND or OE _A = GND and OE _B = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			0.7	1.4	
			V _{IN} = 3.4 V or GND			1	2.4	
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V			1.3	2.6	
			V _{IN} = 3.4 V or GND			3.3	10.6	
C _i						5	10	pF
C _o						9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f₀ = Clock frequency for registered devices, otherwise zero

f₁ = Input signal frequency

N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



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switching characteristics over operating free-air temperature range (see Figure 1)

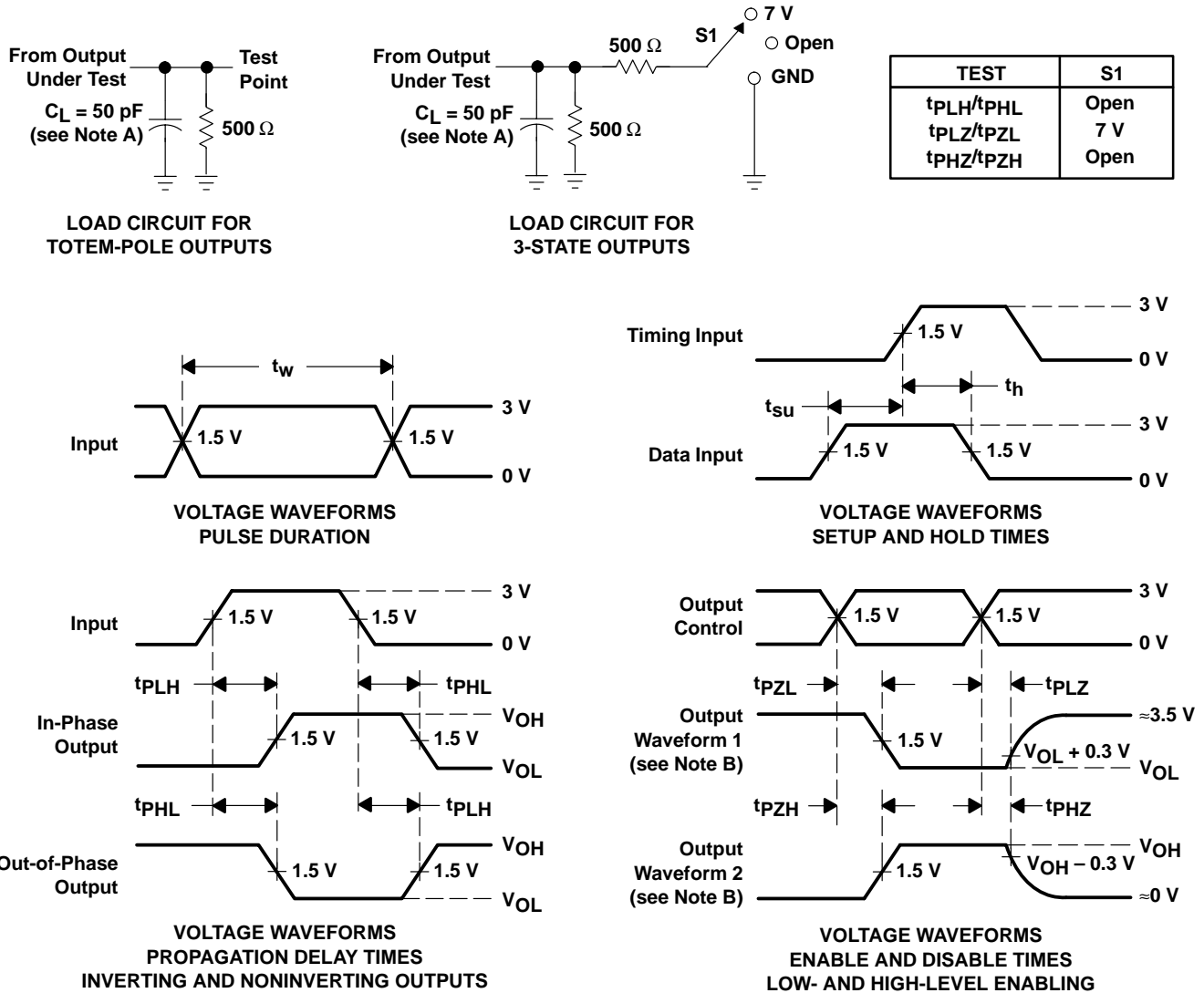
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT541T		CY54FCT541CT		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	8	1.5	4.6	ns
t _{PHL}			1.5	8	1.5	4.6	
t _{PZH}	\overline{OE}	O	1.5	10.5	1.5	6.5	ns
t _{PZL}			1.5	10.5	1.5	6.5	
t _{PHZ}	\overline{OE}	O	1.5	10	1.5	5.7	ns
t _{PLZ}			1.5	10	1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT541T		CY74FCT541AT		CY74FCT541CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	O	1.5	8	1.5	4.8	1.5	4.1	ns
t _{PHL}			1.5	8	1.5	4.8	1.5	4.1	
t _{PZH}	\overline{OE}	O	1.5	10	1.5	6.2	1.5	5.8	ns
t _{PZL}			1.5	10	1.5	6.2	1.5	5.8	
t _{PHZ}	\overline{OE}	O	1.5	9.5	1.5	5.6	1.5	5.2	ns
t _{PLZ}			1.5	9.5	1.5	5.6	1.5	5.2	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9223701M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9223701MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9223705MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CY54FCT541TDMB	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CY54FCT541TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT541ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT541ATPCE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT541ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541ATQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541ATQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541ATSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541ATSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541ATSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541CTQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541CTQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541CTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541TQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT541TQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT541TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT541TSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



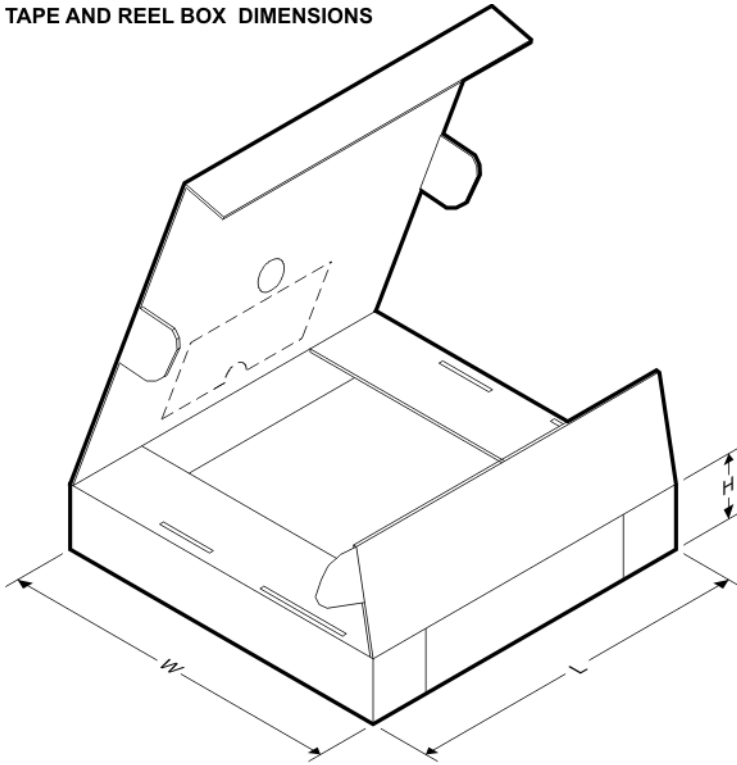
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT541ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT541CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT541TQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT541ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT541ATSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT541CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT541CTSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT541TQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT541TSOCT	SOIC	DW	20	2000	346.0	346.0	41.0

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